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Article

Heterostructured Vertical Organic Transistor for High-Performance Optoelectronic Memory and Artificial Synapse

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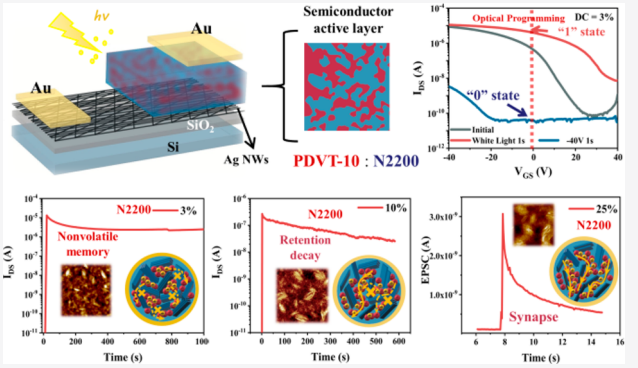
ABSTRACT: Organic field-effect transistor (OFET) memory has received widespread attention due to its easy integration, precise charge modulation, and multi-level memory. However, the performance of organic memory still needs to be improved for its practical application, and the reported technologies are strongly dependent on an additional charge-trapping layer, which increases the complexity of the device. Here, we report a heterostructured vertical organic memory transistor, which uses a p/n semiconductor bulk heterojunction as a semiconductor layer without using any additional charge-trapping layers. The device exhibits a large memory window of 52 V, and the memory ratio reaches 10^5 through electrical operation. Benefiting from the formation of the p/n semiconductor interface and the nanometer-scale transmission length, under the stimulation of visible light, the device achieved a 58 V memory window, high memory ratio 10^5, and retention characteristics of over 10 years, which is better than those of most reported optical organic memory devices. More interestingly, we found that as the level of the doping in the n-type semiconductor increased, the device could transform from nonvolatile memory to artificial synapse, which is associated with the morphology of a heterojunction structure. Hence, we demonstrate a novel technique to manufacture high-performance nonvolatile optoelectronic memory and artificial synapse, which shows great potential in OFET-based memory and neuromorphic devices.



KEYWORDS: *organic transistor, nonvolatile optical memory, vertical channel, artificial synaptic, heterostructure, heterointerface*

INTRODUCTION

With tremendous development of organic materials, organic field-effect transistors (OFETs) have attracted considerable interest in organic electronics due to their characteristics of being lightweight, highly flexible, and easy to fabricate with low cost.[1−14] Although significant advances have been achieved in the planar OFETs, the inherent disadvantage of relatively larger channels and the intrinsically low carrier mobility of organic semiconductors make it difficult to meet the application requirements of high operating frequency and high output current under low operating voltage.[15−17] Compared with that of planar OFETs, vertical organic field-effect transistors (VOFETs) have a much smaller conducting channel length, which is determined by the thickness of the semiconductor (usually tens of nanometers). In a VOFET, the active layer is sandwiched between the mesh source and drain electrodes, and the charge is transmitted through the entire active layer, which is the bulk transmission. Thus, VOFETs aer able to achieve a large current density and high operating frequency under low working voltage, which has attracted widespread attention in the field of electronic devices and has been widely used in various applications, such as photoelectronic memories, artificial synapses, organic light-emitting transistors, and flexible electronic devices.[18−25,44−53]

With the recent emergence of new data-centric electronic applications, a vertical nonvolatile transistor memory shows increasingly significant advantages in various electronic systems due to its unique geometric characteristics. The ultrashort channel enables vertical memory with "write" and "read" faster than that of planar memory, which meets the needs of cutting-edge applications such as human−computer interaction recognition and high-speed sensors.[26,27] Moreover, vertical memory could provide an ultrashort transmission path for photogenerated charges in optoelectronic applications and a stronger electric field to promote separation of the photo-excitons, which reduces the recombination rate of separated photogenerated carriers in the channel and results in the

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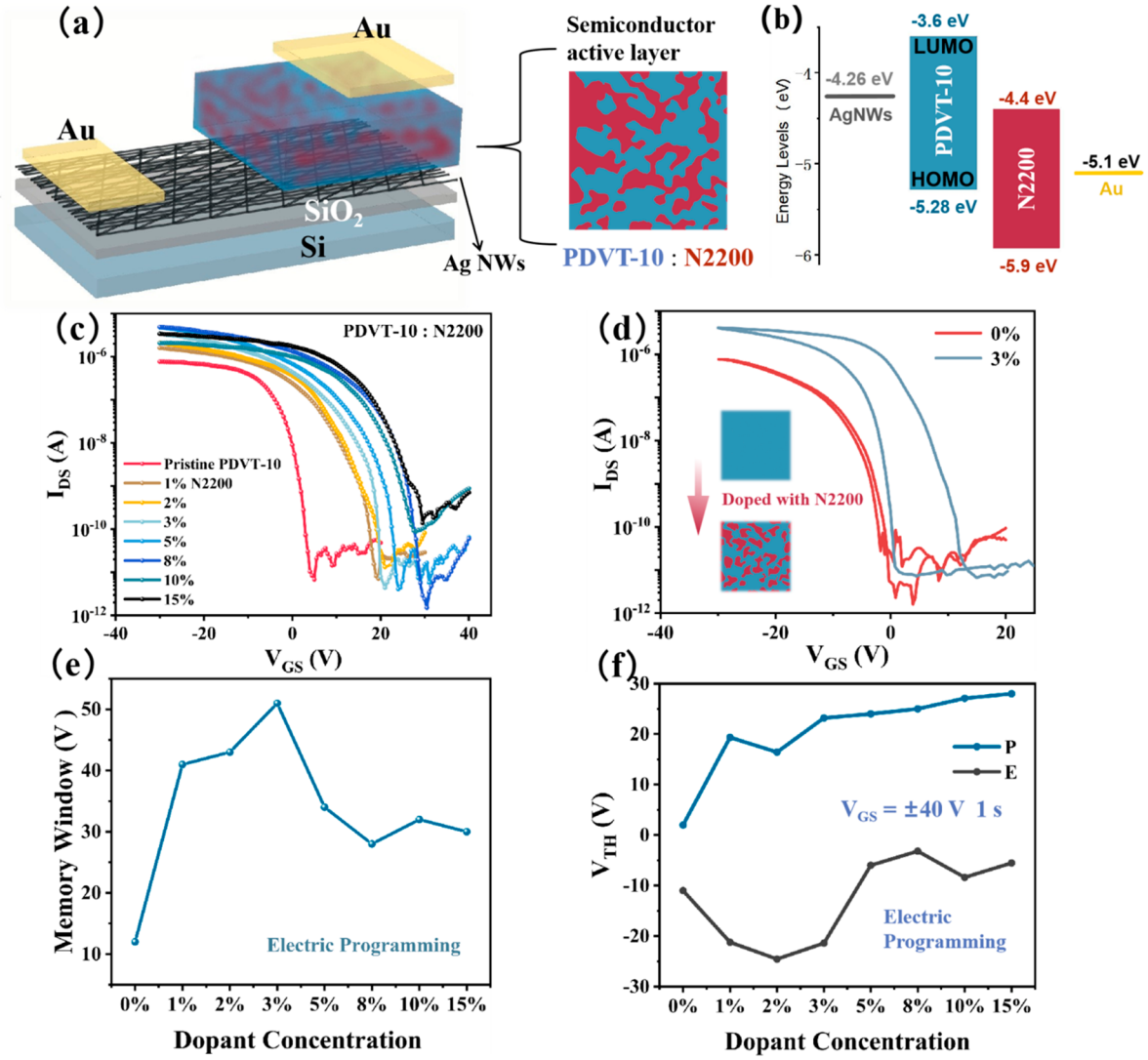

Figure 1. (a) Diagram of the structure of the device. (b) Work function and energy level diagram distribution of Ag nanowires, PDVT-10, N2200, and drain metal Au. (c) Transfer curve of PDVT-10 vertical transistor with different N2200 doping levels. (d) Transfer curves of undoped and doped devices with doping of 3%. $V_{P/E}$ = ±40 V, 1 s electrical pulse to the gate applied for the (e) memory window and (f) threshold voltage for the device with different doping levels.

improvement of capturing efficiency.[28,29] Therefore, the vertical structure can improve the storage efficiency of photoelectronic memory, reduce the power consumption, and be more conducive to realizing multilevel photoelectronic memory. Moreover, a series of transistor memories have been reported in recent research, such as polymer electret memories, ferroelectric polymer memories, and optoelectronic memories.[30−34] Nevertheless, these technologies usually require the charge-storrage layer or other functional layers between the insulation layer and the active layer, which causes many problems. For example, the complex multilayer manufacturing process is required; the floating gate layer will be damaged during the formation of the tunneling layer, and the ferroelectric layer will suffer from fatigue effects. Therefore, it is highly significant to explore novel high-performance organic nonvolatile memories to solve these problems.

Here, we report a heterostructured vertical organic transistor optoelectronic memory in which a p-type/n-type (p/n) semiconductor bulk heterojunction is used as a semiconductor layer without any additional charge-trapping layers and investigate the effect of doping on memory performance. After the n-type semiconductor was doped into the p-type semiconductor, the p/n semiconductor formed a heterointerface that promotes the separation of excitons.[18] At low doping concentrations, discontinuous n-type semiconductors could be used as charge capture centers similar to a quantum well. Under visible light stimulation, the extremely short channel distance and p/n heterointerface would promote the separation and capture of photogenerated carriers, resulting in a large 58 V memory window, high memory ratio of 10^5, and retention characteristics of more than 10 years when mixed with a 3% n-type semiconductor. Interestingly, as the level of doping in n-type semiconductors increases, dispersed n-type semiconductors form a continuous network of n-type channels, which provides a path to electronic transmission, resulting in the leakage of captured electrons. When the doping concentration reached 25%, the device could transform from a nonvolatile memory to an artificial synapse and achieved artificial synaptic functions including postsynaptic current (PSC), short-term memory (STM), and long-term memory

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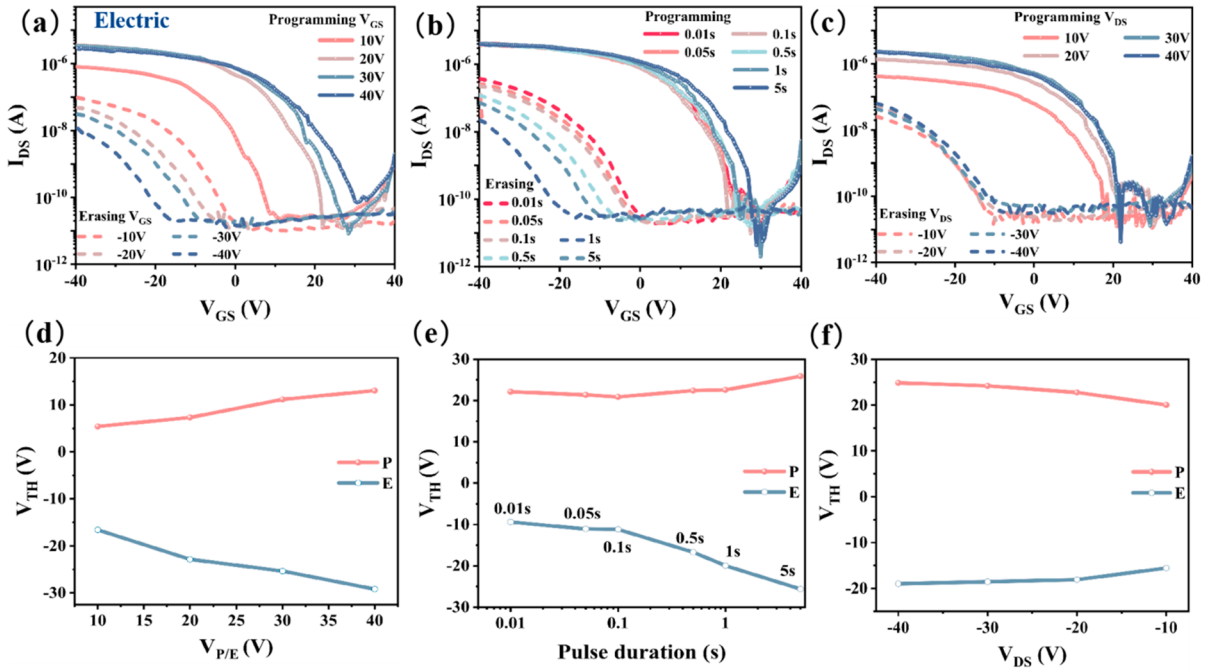

Figure 2. Transfer curve of the memory under different conditions: (a) V_{PE}, (b) pulse duration, and (c) V_{DS}. The memory window of the device under different conditions: (d) V_{PE}, (e) pulse duration, and (f) V_{DS}.

(LTM). Therefore, our devices show great potential in OFET-based optoelectric memory and neuromorphic devices.

RESULTS AND DISCUSSION

Figure 1a showed the configuration of a vertical memory device based on a doped heterostructure semiconducting layer without any extra charge-storage layer. Doped heterostructure blends composed of p-type and n-type organic semiconductors, poly[2,5-bis(2-decyltetradecyl)pyrrolo[3,4-*c*]-pyrrole-1,4(2*H*,5*H*)-dione-*alt*-5,5″-di(thiophen-2-yl)-2,2″-(*E*)-2-(2-(thiophen-2-yl)vinyl)thiophene] (PDVT-10) and poly-{[*N*,*N*′-bis(2-octyldodecyl)naphthalene-1,4,5,8-bis-(dicarboximide)-2,6-diyl]-*alt*-5,5′-(2,2′-bithiophene)} (N2200), respectively, were employed as the semiconductor layer. N2200 has good solubility and high electron affinity in common organic solvents, whereas PDVT-10 has high mobility and good environmental stability. Therefore, we first chose N2200 and PDVT-10 to mix. After being mixed, the two materials can form a suitable energy band relationship, which is conducive to trapping and storing charges. The Si was used as the gate, and SiO_2 was used as the insulating layer; the silver nanowires were used as the mesh source electrode, and the thermally evaporated gold was used as the source and drain electrodes. Materials and fabrication are shown in the Experimental Section. The energy level diagram is shown in Figure 1b.

First, the impact of the concentrations of N2200 on transistor performance was studied, as shown in Figure 1c. It showed that as the proportion of N2200 doped into PDVT-10 increases, the turn-on voltage (V_{ON}) of the transistor gradually shifts in the positive direction from around 0 V. It is worth noting that the on-state current (I_{ON}) and switching ratio (I_{ON}/I_{OFF}) of the transistor increased when a small amount (1−8%) of N2200 was added, along with the decrease of the off-state (I_{OFF}) current. However, when the doping concentration was higher (10−15%), I_{OFF} obviously increased along with the decrease of the switch ratio. This indicated that adding a small amount of N2200 to PDVT-10 can enhance transistor performance, whereas with a further increase of the doping ratio of N2200, the performance of the transistor would be degraded. Figure 1d shows the double-sweep transfer curve of the pure PDVT-10 film device and a device doped with 3% N2200. It can be observed that the transistor has a larger hysteresis window of 12 V after being doped with N2200, and the hysteresis window of the undoped device is 0.5 V, which indicates the potential of the device for memory applications. In this work, the doping concentration is defined according to the ratio of N2200 to the total mass. Therefore, the memory performance after being doped with different proportions of N2200 was then investigated. Under the fixed V_{DS} = −40 V, the gate voltage pulse (V_{GS} = ±40 V, 1 s) was applied to realize the "programming" and "erasing" operation. The threshold voltage (V_{TH}) and the memory window of the device at different doping levels are shown in Figure 1e,f, exhibiting the largest memory window of 52 V with a doping concentration of 3%. In order to further study the effects of the doping ratio, the morphology of different blending films was investigated by atomic force microscopy. As shown in Figure S6a, the pure PDVT-10 film was smooth with a low roughness. When the doping ratio was 3%, discontinuous N2200 areas were observed in Figure S6b. With the increase of doping concentration, the blending film exhibited larger roughness, which induced more charge-trapping sites. Further, the dispersed N2200 gradually became continuous areas with high roughness as the degree of doping increases, as shown in the Figure S6h.

Moreover, appropriate gate pulses ($V_{P/E}$) were applied to the device for programming or erasing operations to further investigate the memory characteristics, as presented in Figure 2a,d. The shift of the transfer curve under different gate voltages indicated that the trapping density of charges in the channel was controllable. Figure 2b,e shows the effect of pulse

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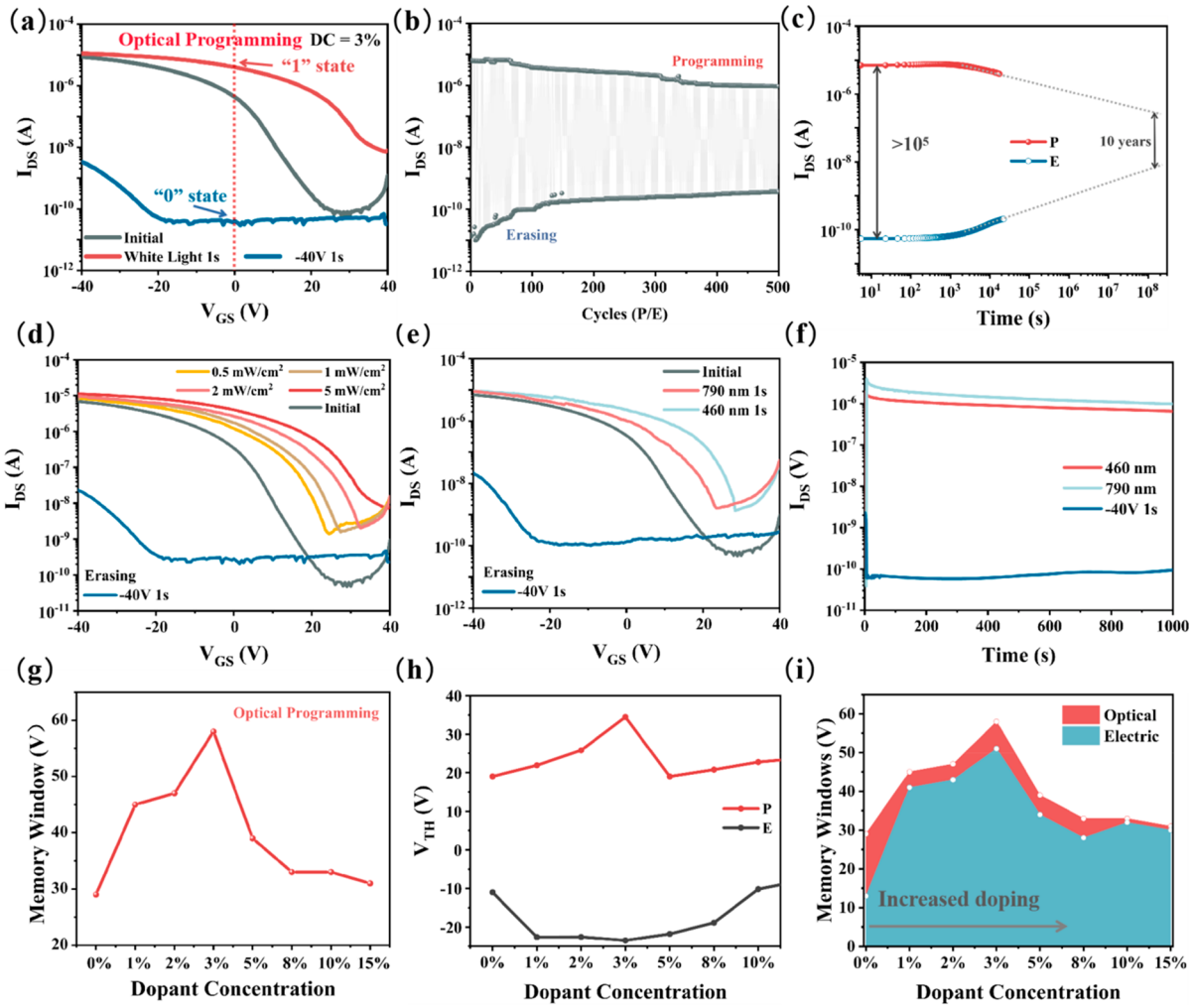

Figure 3. (a) Transfer curves of the photoelectronic memory after optical programming (white light, 5 mW cm^{-2}, 1 s) and electrical erasing (dark, V_{GS} = −40 V, 1 s). (b) Endurance characteristics of the device in 500 cycles of PRER. (c) Retention characteristics of photoelectronic memory after optical programming and after electrical erasing. (d) Transfer curves of the device by different intensity white light programming and (e) wavelength light pulse (460 and 790 nm) programming. (f) Retention characteristics of the device with light programming (460 and 790 nm, 1 s). (g) Memory window and (h) threshold voltage for the device with different doping levels. (i) Memory window of the stimulus source with gate electric pulse (−40 V, 1 s) and white light pulse (5 mW/cm^2, 1 s) under different doping concentrations.

duration on the memory window and demonstrates that the memory window increased with the increase of pulse duration. Figures 2c,f shows the impact of different V_{DS} on memory performance, indicating that V_{DS} directly affects the memory ratio (I_{ON}/I_{OFF}) and has a negligible impact on memory windows. In addition, the endurance and retention characteristics of the memory are shown in Figure S7a,b. The device retention was good with a high memory ratio of 10^4 after 10^4 s and still maintained a high memory ratio of 10^5 after 500 cycles of programming−reading−erasing−reading (PRER).

In order to further explore the role of doped N2200 in memory applications, the influence of light illumination on optical memory function of the device was investigated. As shown in Figure 3a, V_{TH} moved forward after being stimulated by the white light pulse, indicating that a small amount of N2200 mixed with PDVT-10 can be used as a trapping site for electrons. Afterward, the holes were injected from PDVT-10 into the N2200 to neutralize the electrons after the negative pulse was applied, resulting in V_{TH} being moved negatively. Consequently, the device achieved a large memory window of 58 V and a high memory ratio of 10^5. The device also showed excellent endurance and retention characteristics, as shown in Figure 3b,c, respectively. The multilevel memory function of the device can be simply modulated by different light intensities and wavelengths, as shown in Figure 3d−f. In addition, the memory window of devices doped with different proportions of N2200 were also investigated, and the maximum memory window was observed when the doping proportion was 3%, as shown in Figure 3g−i. The key characteristics of the organic transistor memory in this work compared with those of other reported works are summarized in Table S1, which shows that the performance of the memory was better than most reported works with traditional processes and structures. In addition, we also tested the relative performance of the planar structure device based on the same manufacturing conditions, as shown in Figure S8, which showed that the vertical structure can create a larger optical storage window. Devices based on other hybrid semiconductor films were also manufactured and measured to investigate whether this system was suitable for other organic semiconductors,[26,30,38−43] as shown in Figure S10. After being

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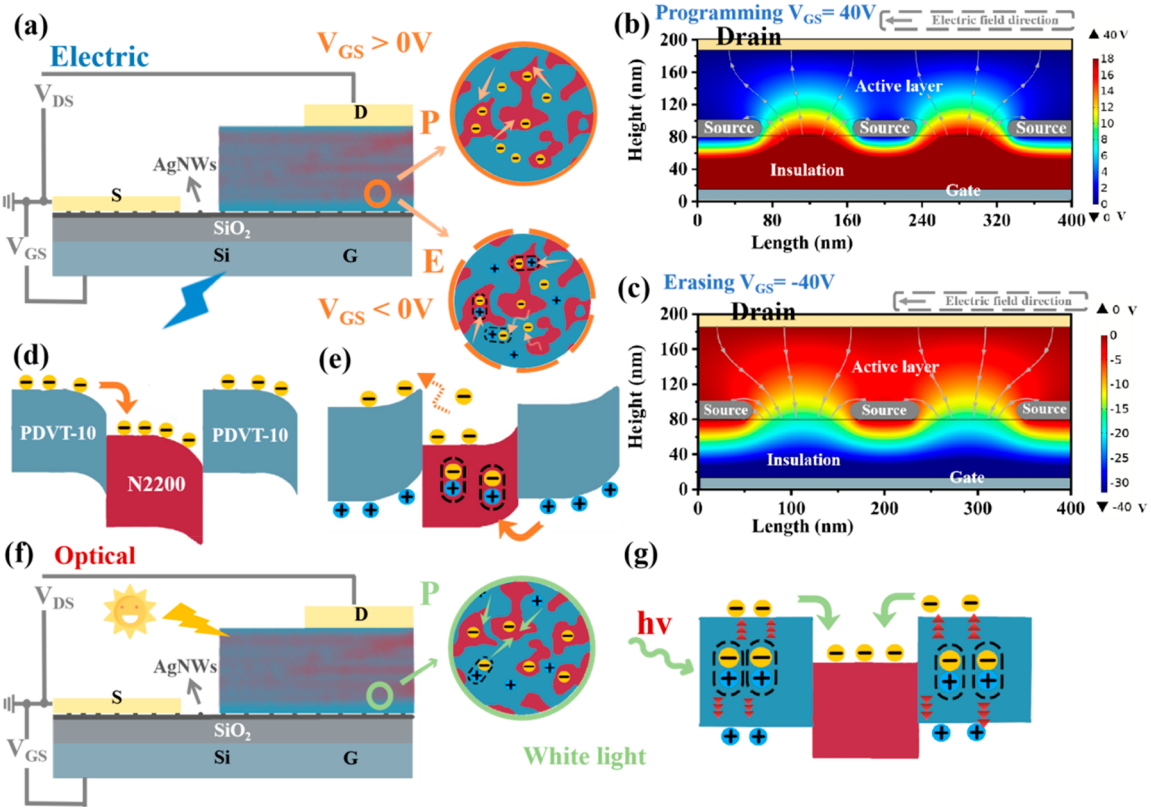

Figure 4. Schematic illustrations of the mechanism of the memory. (a) Schematic diagram of the device and charge movement during electric programming and electric erasing. (b,c) Distributions of electric potential within the active and insulation layer of the memory structures (V_{DS} = −40 V, the source was grounded) through semiconductor physics simulations. The simulations were performed by considering V_{GS} with (b) +40 V and (c) −40 V. Schematic diagram of energy band bending during (d) electric programming and (e) electric erasing. (f) Schematic diagram of the device and charge movement during optical programming. (g) Schematic diagram of energy band during (d) optical programming.

doped, all devices had a large memory window, which proved the versatility of the system.

The working mechanism of the memory is shown in Figure 4. COMSOL Multiphysics was used to simulate the electric field distribution and carrier concentration distribution in the memory device under different conditions to analyze the transfer process of charge in the channel, as presented in Figures S15−S18. When applying a positive V_{GS} for programming, as presented in Figure 4b, the electric field in the channel was transferred from the source to the drain. The electrons in the channel moved against the direction of the electric field and accumulated at the interface between the insulator and the semiconductor layer, as presented in Figure S16. As the N2200 was doped into PDVT-10, the heterostructure of PDVT-10/N2200/PDVT-10 formed a barrier similar to a quantum well,[35−37] allowing parts of the electrons in the channel to be trapped and stored in discontinuous N2200, as shown in Figure 4d. As a result, the electron concentration in the channel decreased and the V_{TH} of the device shifted in the positive direction. When a negative V_{GS} was applied, as shown in Figure 4c, an excess number of holes were stored in discrete N2200 during the process of transporting along the electric field, as shown in Figure 4e. Consequently, the transfer curve moved negatively, and a larger memory window appeared. To further verify the trapping/detrapping of charge, the surface potential of the device was investigated by Kelvin probe force microscopy (KPFM) after programming/erasing, as shown in Figure S20. After being programmed, the surface potential of the film increased, whereas the lower surface potential was observed after erasing. Generally, the increase of the hole concentration or decrease of the electron concentration would lead to the surface potential increase, so the results of changes in surface potential confirmed the trapping/detrapping of charges.

Moreover, the mechanism of the optoelectronic memory is discussed in Figure 4f. During visible light programming, the PDVT-10 absorbed the photons and produced photoexcitation in the channel. As the PDVT-10 has a higher LUMO, photoelectrons were more easily transferred to the N2200, while photoholes accumulated in the PDVT-10, as shown in Figure 4g. Moreover, the holes were injected from PDVT-10 into the N2200 after applying negative V_{GS}, causing the trapped electrons to be erased. As a result, the nonvolatile memory functions and a large memory window were achieved. The surface potential of the device during operation was measured by KPFM, as shown in Figure S21. The surface potential increased after optical programming and decreased after erasing, which verified the trapping/detrapping of charges with optical programming.

Interestingly, it was found that as the proportion of N2200 incorporated increased, the nonvolatile characteristics of the memory gradually degraded. When the proportion of doped N2200 increased to 25%, the device lost nonvolatile memory behavior and exhibited the behavior of a synaptic transistor. Therefore, the synaptic transistor characteristic of the device under higher doping concentration was investigated. In human neural networks, the synapses, an important element in the transmission of information in the human body, are

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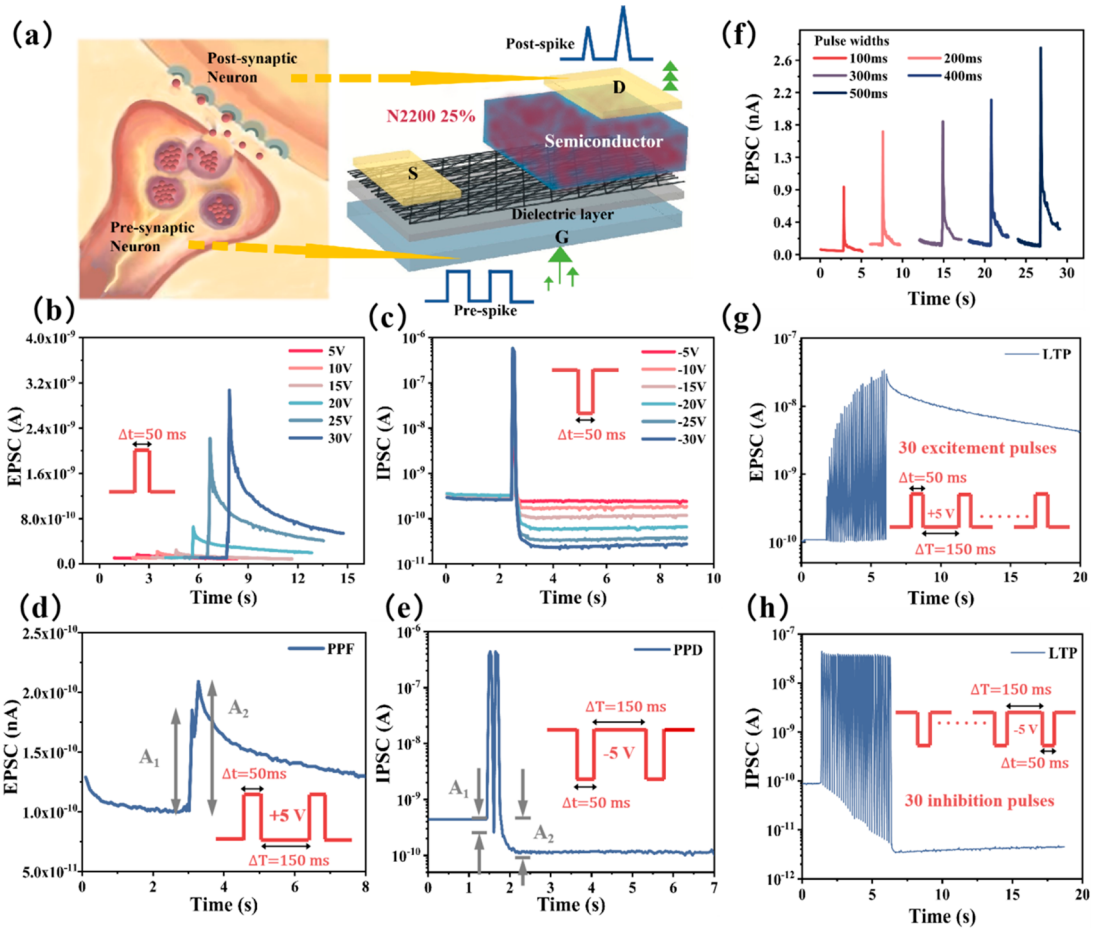

Figure 5. (a) Schematic diagrams of biological synapses and electrical stimulation synaptic memory devices. (b) When doped with 25% concentration of N2200, the device obtains EPSC behavior under different amplitude voltage pulses. (c) Device obtains IPSC behavior under different amplitude. (d) After a pair pulse with V_{GS} = +5 V, a pulse interval = 150 ms, and a pulse width = 50 ms were applied, the PPF of the N2200-doped device was induced. (e) After a pair gate pulse with V_{GS} = −5 V, $T_{interval}$ = 150 ms, and t_{width} = 50 ms were applied, the PPF of the N2200-doped device was induced. (f) the device obtains EPSC behavior under different widths voltage pulse. (g−h) Electrical potentiation (t_{width} = +5 V, $T_{interval}$ = 150 ms, t_{width} = 50 ms) and suppression (V_{GS} = −5 V, $T_{interval}$ = 150 ms, t_{width} = 50 ms) triggered by 30 pulses.

responsible for connecting the axons of the former neuron to the dendrites of the latter neuron, as shown in Figure 5a. When the presynaptic membrane receives an electrical signal, the synaptic vesicle that covers the neurotransmitter is formed in the cell membrane. The synaptic vesicle transmits neurotransmitters to the postsynaptic, causing resistance change between the previous and the latter cell membrane, which regulated synaptic plasticity and completed biological learning and memory behavior. To simulate artificial synapse, the synaptic plasticity of the device with 25% doping concentration were investigated by applying different gate pulses, as shown in Figure 5b,c. After a positive gate pulse was applied, the output current of the device suddenly increased and then decayed to its initial value in a short period of time, which was excitatory PSC (EPSC). In contrast, the generated inhibitory PSC (IPSC) exhibited an output current lower than that of the initial value after applying a negative gate pulse. The PSC intensity increased as the pulse amplitude increased and then returned to the initial value within seconds, which is a characteristic of the spike amplitude-dependent plasticity of synaptic transistors. Moreover, paired-pulse facilitation (PPF) and paired-pulse depression (PPD), which are typical forms of STM of artificial synapses, were investigated to further explore the synaptic plasticity of the device, as shown in Figure 5d,e. The results showed that the synaptic plasticity of the device can be adjusted through different pulse stimuli. Pulses of different widths were used to train the intensity of EPSC, as shown in Figure 5f, suggesting that increasing the pulse width of the stimulus pulse can significantly regulate synaptic plasticity. To investigate the transition of the device from STM to LTM, 30 consecutive V_{GS} pulses were applied. Figure 5g,h exhibits the EPSC and IPSC triggered by 30 pulses, respectively, suggesting that the device can transform from STP to LTP through repeated stimulation and has the ability to learn and remember.

Unlike most reported organic synaptic transistors, the synaptic transistor in this work does not rely on any charge-trapping layers, while it is achieved by adding N2200 with a higher concentration to PDVT-10. As presented in Figure 6a,d, when a small amount of N2200 (3%) was incorporated, the N2200 formed discrete and independent trap sites in PDVT-10. Under the influence of an electric pulse, the system of PDVT-10/N2200/PDVT-10 formed barriers similar to quantum wells to trap and store electrons, showing stable memory retention characteristics. However, as shown in Figure 6b,e, with the increase of the proportion of N2200 (10%), a large amount of N2200 formed locally a continuous network structure that provided a path for the transfer of electrons,

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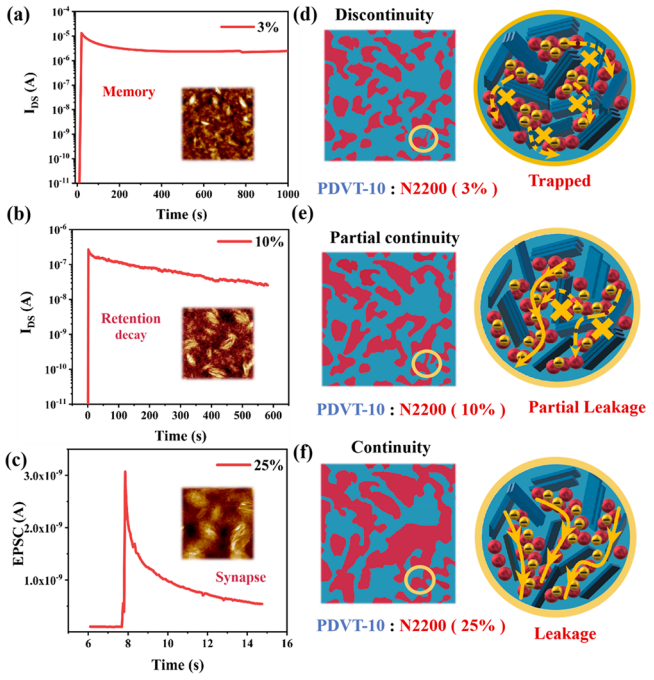

Figure 6. (a) When a low doping concentration (3%) is applied, a voltage stimulus is applied, and the device exhibits a nonvolatile memory behavior. (b) When the doping concentration increases (10%), the retention characteristics will decay. (c) When a high concentration (25%) is applied, a voltage stimulus is applied, and the device exhibits a synaptic behavior. (d–f) As the concentration increases, N2200 gradually forms a continuous network structure in PDVT-10, resulting in leakage of trapped charges.

which caused the leakage of the stored charge and the retention characteristics of the device degraded. When the doping concentration was further increased to 25%, as shown in Figure 6c,f, excess N2200 formed a large number of continuous network structures. Therefore, when a positive pulse was applied, electrons were trapped in the N2200 area and output current increased rapidly. However, the excessively doped N2200 formed more network structures for electron transporting, resulting in more charge leakage and faster output current decay. As a result, the device exhibited the EPSC behavior. After a negative pulse was applied, the holes were transferred from PDVT-10 to N2200 and the concentration of electrons in the channel increased, resulting in a decrease in the output current, which was IPSC.

CONCLUSION

In summary, we propose a heterostructured vertical organic transistor. Due to the use of a bulk heterojunction and vertical structure, the device could provide an ultrashort transmission path for photogenerated charge. Therefore, it exhibits excellent nonvolatile memory function under visible light radiation with a memory window of 58 V and retention characteristics of more than 10 years, which is competitive or better than recent traditional organic optoelectronic transistor memory. Interestingly, as the concentration of the n-type semiconductor increases, dispersed n-type semiconductors form a continuous network of n-type, which provides a path to electronic transmission, resulting in the loss of captured electrons. Moreover, with a further increase of the doping concentration, the device could transform from nonvolatile memory to artificial synapse. Therefore, our results provide a new strategy for realizing high-performance organic transistor memory and demonstrate the application potential of this strategy in neuromorphic devices.

EXPERIMENTAL SECTION

Materials and fabrication. The original solution of silver nanowires (5 mg/mL in isopropyl alcohol) was purchased from Suzhou Cold Stone Nano Material Technology Co. In this work, the concentration of the silver nanowire solution used was optimized and diluted to 0.5 mg mL^{-1} using isopropyl alcohol. Before the solution was mixed, the PDVT-10, IDTBT, DPPDTT, ITIC, and N2200 semiconductors used in the experiment were dissolved in chlorobenzene with a concentration of 5 mg mL^{-1}, and then the p-type semiconductor solution was mixed with the n-type semiconductor solution at different concentrations. The Si/SiO_2 (100 nm) substrates were first cleaned with acetone and then washed for 30 s in turn with isopropyl alcohol, trichloromethane, and deionized water; the cleaning process was cycled three times and eventually dried with N_2 gas. Afterward, the optimized silver nanowire solution (0.5 mg mL^{-1}) was spin-coated at 2000 rpm for 60 s on the cleared SiO_2 and annealed at 120 °C for 13 min to form a mesh source electrode. After the semiconductor solution was mixed in a certain proportion, the mixed solution was spin-coated on the mesh source electrode at 1000 rpm for 60 s in a nitrogen glovebox and finally annealed at 150 °C for 10 min to form an active layer. The sample was partially immersed in chloromethane to dissolve the unwanted active film and expose the source electrode. Finally, 50 nm gold was thermally evaporated onto the naked mesh source electrode and active layer through the shadow mask as the source electrode and drain electrode. The effective channel area of vertical transistors is mainly determined by the overlapping area of the mesh source electrode and the drain electrode. Effective channel area was 200 μm × 200 μm, as measured with a microscope.

Measurement. The electrical performance was characterized by a semiconductor parameter analyzer (Keysight B2902A). The atomic force microscope (Nanoscope III, Veeco Instruments, Inc.) was used to measure the morphology of the mixing films under ambient conditions. UV–vis absorption was used to characterize the ultraviolet–visible–near-infrared spectra (Shimadzu UV-3600 Plus).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsphotonics.1c01167.

Thickness of the mixed film (Figure S1); topography of Ag nanowire source (0.5 mg/mL) (Figure S2); memory window of the memory at different mixing ratios (Figure S3); 500-cycle double-swept transfer curve of the vertical transistor (Figure S4); transfer curve of 115 doped (3%) organic vertical transistors (Figure S5); surface roughness of the blending film with different doping ratios (Figure S6); endurance and retention characteristics of the device (Figure S7); transfer curve of undoped device under electrical/optical operation (Figure S8); memory window of the planar memory (Figure S9); transfer curve of optoelectronic memory with different doping ratios (Figure S10); UV–vis absorption of PDVT-10 film, N2200 film, and mixing film with doping 3%

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N2200 (Figure S11); molecular structure of PDVT-10, DPP-DTT, IDTBT, and N2200 (Figure S12); memory window of memory devices based on different blending systems (Figure S13); transfer curves of different semiconductor (Figure S14); potential distribution and the charge concentration distribution of the device under different operating conditions (Figures S15−S18); capacitance of doped film (3%) and undoped film (Figure S19); KPFM image of the doping film (Figures S20 and S21); PSC of the device (Figure S22); dependence of PPF and PPD ratio of the device and on various pulse intervals (Figure S23); surface potential of mixed thin films with different doping concentrations (Figure S24); Transfer curve and retention of devices with 50% doping concentration (Figure S25); comparison of organic field-effect memory characteristics based on different mechanisms (Table S1) (PDF)

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Notes

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