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Self-calibrating programmable photonic integrated circuits

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Programmable photonic integrated circuits (PICs) are dense assemblies of tunable elements that provide flexible reconfigurability to enable different functions to be selected; however, due to manufacturing variations and thermal gradients that affect the optical phases of the elements, it is difficult to guarantee a stable correspondence between the electrical commands to the chip, and the function that it provides. Here we demonstrate a self-calibrating programmable PIC with full control over its complex impulse response, in the presence of thermal cross-talk between phase-tuning elements. Self-calibration is achieved by: (1) incorporating an optical reference path into the PIC; (2) using the Kramers–Kronig relationship to recover the phase response from amplitude measurements; and (3) applying a fast-converging self-calibration algorithm. We demonstrate dial-up signal processing functions with complex impulse responses using only 25 training iterations. This approach offers stable and accurate control of large-scale PICs, for demanding applications such as communications network reconfiguration, neuromorphic hardware accelerators and quantum computers.

Photonic integrated circuits (PICs)[1–5], formed by dense discrete integrated optical elements, offer ultra-broad analogue bandwidths that could complement digital electronics and enable throughputs up to tens of petabits per second. Meanwhile, subject to the relatively long design-fab-packaging-test iterations of up to two years[6], PICs are evolving towards programmable architectures (in parallel with application-specific architectures) that enable diverse signal processing functions to be realized within a single chip[7–10]. As such, programmable PICs can dramatically accelerate the development of photonic circuits and have enabled a wide range of applications such as optical communications[11], optical signal processing and computing[12–18], quantum computing[19] and artificial intelligence hardware[20].

The characteristics or system functions of PICs are defined by their transfer functions (that is, phase and amplitude frequency responses) or temporal impulse responses. Due to the difficulties in maintaining sub-wavelength accuracies during fabrication, adaptive post-production tuning of on-chip parameters—such as the power splitting ratio of the couplers and the phase shifts—is necessary to guarantee a desired frequency response being dialed up on command. As the complexity of PICs increases, the difficulty of programming them—due to manufacturing variations and the dynamics of thermal cross-talk[21,22]—becomes overwhelming, thus limiting their practicality, particularly in scenarios when a guaranteed performance is required within milliseconds of a command change (for example, in a telecommunications network).

Machine learning algorithms have recently offered routes towards mitigating the complex effects of on-chip cross-talk. Successful demonstrations have been implemented using: hexagonal waveguide meshes[23], coupled micro-ring resonators[24–30], optical switches and interferometer arrays[31–35]. However, these programmable PICs have yet to achieve the full control of their complex-valued characteristics (that is, both the amplitude and phase frequency responses) and thus face challenges in achieving one or more of: (1) guaranteed operation at more than one single wavelength, which would increase processing bandwidth[31–33,35]; (2) simultaneous manipulation of both the phase and amplitude frequency responses for versatile signal processing functions[24–30,34]; and (3) fast convergence during learning, within tens of iterations instead of thousands of iterations. One of the major challenges is accurately measuring a PIC's phase response, due to phase variations in the measurement paths (such as coupling fibres), and the inaccuracies (optics) or limited bandwidths (electronics) of the measurement instrument.

Here we demonstrate a self-calibrating programmable PIC with full control of the complex-valued impulse response over bandwidths of several hundred gigahertz. Its basic structure is a finite impulse response (FIR) filter with adjustable phase and amplitude taps. The process for setting the tap weights requires: (1) an integrated reference path that establishes an on-chip Kramers–Kronig relationship[23,36–41]; (2) recovery of the phase response from an amplitude-response measurement using a tunable laser and photodiode; (3) Fourier transformation of this, to determine the complex-valued impulse response; and (4) a self-calibration algorithm to determine the tap-value errors from the measured and desired impulse responses. We demonstrate that the self-calibration algorithm can compensate for thermal cross-talk without the need of prior knowledge of the chip, which may include: random manufacturing phase errors, the electrical currents required for a given phase change of the thermal phase shifters, and their resistances. The FIR structure of the PIC is versatile, enabling distinctive signal processing functions to be programmed on demand. Our self-calibrating integrated photonic signal processor represents a major step towards realizing PICs that can quickly provide a guaranteed programmable transfer function over a broad optical bandwidth. This is essential for real-time signal processing applications

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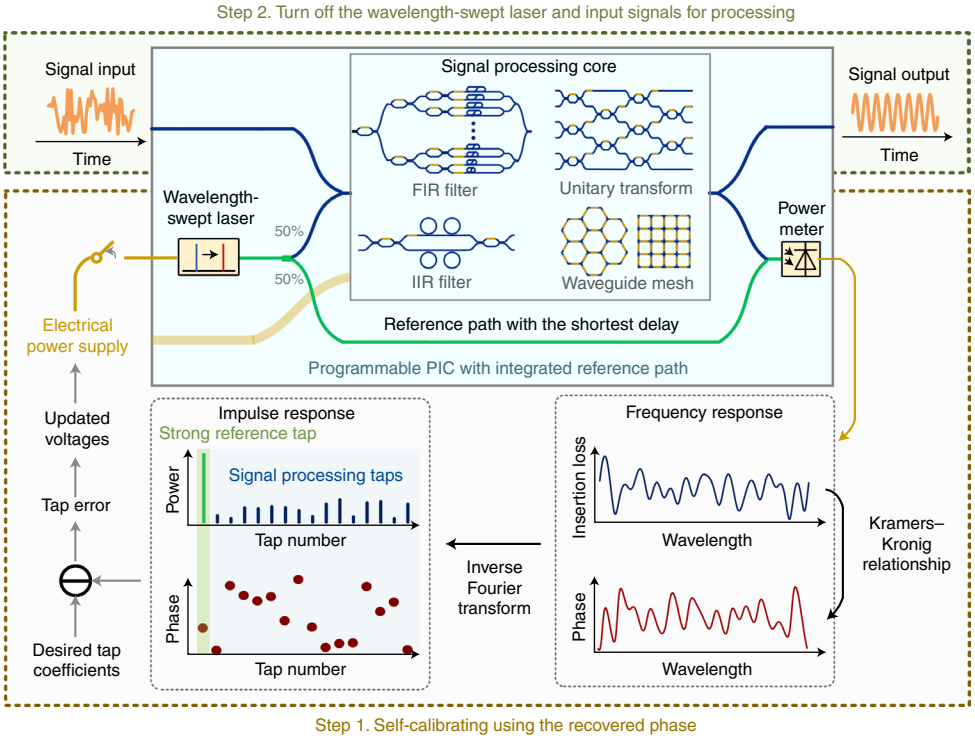

Fig. 1 | Conceptual diagram of the self-calibrating integrated broadband PIC. In our PIC design (blue shaded region), a reference path (green) is added around the signal processing core with the top input/output ports accessing the signal processing core and the lower ports coupled to a tunable laser and photodiode for self-calibration. The calibration uses the Kramers–Kronig relationship to find the phase from the intensity spectrum, then an inverse Fourier transform to find the powers and phases of the signal processing tap weights, which then inform the update procedure.

such as communications channel equalization, image processing and optical neural networks.

Results

The self-calibrating programmable PIC. As shown in Fig. 1, the self-calibrating PIC consists of a signal processing core coupled in parallel with a reference path that has the shortest delay on the chip. The signal processing core, with a frequency response of $H_{spc}(\omega)$ (where ω is the angular frequency) can be implemented in diverse forms such as FIR filters, infinite impulse response filters, unitary transformers and waveguide meshes[10]. The operation of the self-calibrating PIC consists of two steps. In the first step, the chip is self-calibrated, during which the insertion loss (that is, square of the amplitude response) of the whole chip is measured with a wavelength-swept laser and an optical power meter—via the optical ports accessing both the signal processing core and the reference path—to recover the phase response and thus the impulse response. In the second step, the wavelength-swept laser is switched off, and the signals to be processed are input and output at the optical ports that access the signal processing core trained for specific applications. Due to the separated pairs of ports for calibration and signal processing, the reference path does not impose any limitations on the signal processing core's transfer function. This phase recovery method is capable of recovering the phase response of generic two-port integrated photonic devices such as FIR and infinite impulse response filters (see Supplementary Information for more simulated cases), with a minor increase of complexity and footprint (two additional couplers and one reference path, resulting in an increase of footprint $<3\,mm^2$). Furthermore, by introducing progressively delayed coupling paths (Supplementary Information), this method can be tailored to measure and calibrate multi-port devices such as the universal multi-port interferometer, with a reasonable increase of complexity and footprint.

The Kramers–Kronig relationship is used to recover the phase response from the amplitude response, but requires the minimum phase condition to be met[36]; this can be achieved by adding a strong impulse at the beginning of the original impulse response. The frequency response of the entire chip, including the reference path, can be given as $H_{chip}(\omega)=H_{ref}(\omega)+H_{spc}(\omega)e^{j\omega\tau}$, where $H_{ref}(\omega)=h_{ref}$ and $\tau>0$ (h_{ref} denotes the amplitude and phase of the reference tap). The necessary and sufficient minimum phase condition of the Kramers–Kronig relationship is that the on-chip system $H_{chip}(\omega)$ and its inverse are both causal (that is, the zeros and poles are all inside the unit circle); this corresponds with a regulation onto the strength (intensity) of the reference tap as $|h_{ref}|>|H_{spc}(\omega)|$ (see Supplementary Information for the proof), which can be guaranteed by using 3 dB (50% to 50%) couplers to equally split the input optical power between the reference path and the signal processing core, and recombine the paths. As the reference path has the shortest path and thus the lowest optical loss, the minimum phase condition is met. Furthermore, we note that the 3 dB coupler achieves the optimum optical power ratio between the reference path and the signal processing core, as it maximizes the signal processing core's intensity $|H_{spc}(\omega)|$ while guaranteeing the minimum phase condition, thus reducing the impact of insertion loss inaccuracies brought about by the measurement instruments (Supplementary Information).

The chip's phase response can be recovered from the amplitude response as $\log\left(\left|\widehat{H_{chip}(\omega)}\right|\right)$, where $\left|\widehat{H_{chip}(\omega)}\right|$ denotes the Hilbert transform of $|H_{chip}(\omega)|$. The impulse response of the whole chip h_{chip}, including the reference path, can be obtained with an inverse Fourier transformation and then compared with the desired impulse response to find an array of errors for the subsequent training process. The integrated reference offers a compact and stable solution for on-chip phase recovery in programmable PICs;

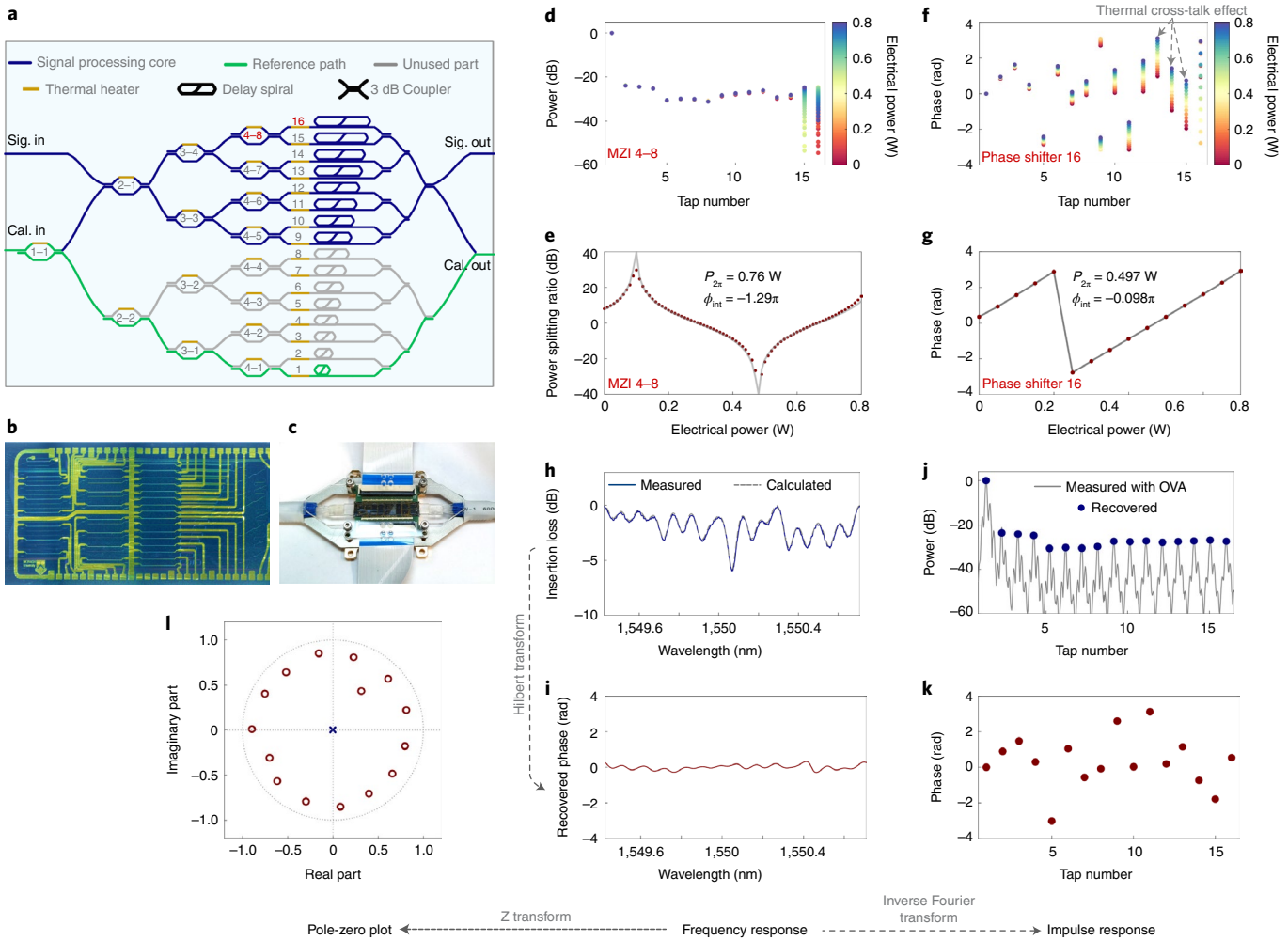

Fig. 2 | Experimental results for on-chip Kramers–Kronig phase recovery. a, Illustration of the 16-tap FIR chip's layout. The top pair of ports is for signal (Sig.) input and output, whereas the bottom pair of ports is for calibration (Cal.). **b**,**c**, Photos of the fabricated chip (**b**) (where the inset is the cross-section of the waveguide using a double-stripe geometry) and the packaged device (**c**). **d**–**g**, Measured powers of the 16 taps (**d**) and the power splitting ratio of MZIs 4–8 (**e**), with electrical power applied onto MZIs 4–8 sweeping from 0 to 0.8 W. Measured phases of the 16 taps (**f**) and the phase of phase shifter 16 (**g**), with electrical power applied onto phase shifter 16 sweeping from 0 to 0.8 W. **h**, The measured insertion loss spectrum of a certain configuration of the tap coefficients. **i**, The phase response recovered via Hilbert transform. **j**,**k**, Power (**j**) and phase (**k**) of the impulse response or tap coefficients recovered from inverse Fourier transform of the frequency response, or measured using an OVA. **l**, Poles and zeros recovered via a Z-transform of the frequency response.

external reference paths using either free-space or fibre components will substantially increase the system's complexity and size, and are subject to temperature or stress fluctuations of the external environment that can greatly deteriorate the accuracy of phase recovery. Due to the capability of obtaining the full frequency response of the chip, the on-chip parameters can be directly measured and trained, thus enabling fast convergence of the training process.

Kramers–Kronig phase recovery. For a proof-of-concept demonstration, we employed a 16-tap FIR chip for pulse processing[42], with the shortest path as the reference path and half of the taps as the signal processing core (Fig. 2). Note that the taps denoted by waveguide paths in grey lines—although needed to be manipulated in power (that is, minimizing the optical power in the unused paths) in this proof-of-concept demonstration—were not used for signal processing, as they cannot be accessed by the on-chip ports without interfering with the reference tap, and thus could be removed in future implementations. The upper pair of on-chip ports, accessing the 8-tap signal processing core, was used as the signal input and output, whereas the lower pair of on-chip ports, accessing the 16-tap FIR filter, was used for phase recovery and the self-calibration process. Here we set the reference path to have a high intensity to guarantee the minimum phase condition with a one-shot setting process (Methods).

Figure 2h shows the power response of the 16-tap filter at a certain configuration for phase recovery verification, where the intensities of the 8-tap signal processing core were roughly set as equal, and the phases were random without electrical power applied. By recovering the phase information (Fig. 2i) from the amplitude response (the square root of the insertion loss spectrum) via a Hilbert transform, the full information of the 16-tap FIR filter can be recovered, including the phase response, the amplitudes and phases of the tap coefficients (Fig. 2j–k), and the zeros and poles of the filter (Fig. 2l).

The applied electrical powers to the signal processing core's tunable Mach Zehnder interferometers (MZIs) and phase shifters were swept from 0 to 0.8 W, sequentially, to characterize the initial phase shifts (ϕ_{int}) and the power ($P_{2\pi}$) needed to achieve 2π phase shifts (Fig. 2d–g and Supplementary Information). The randomness

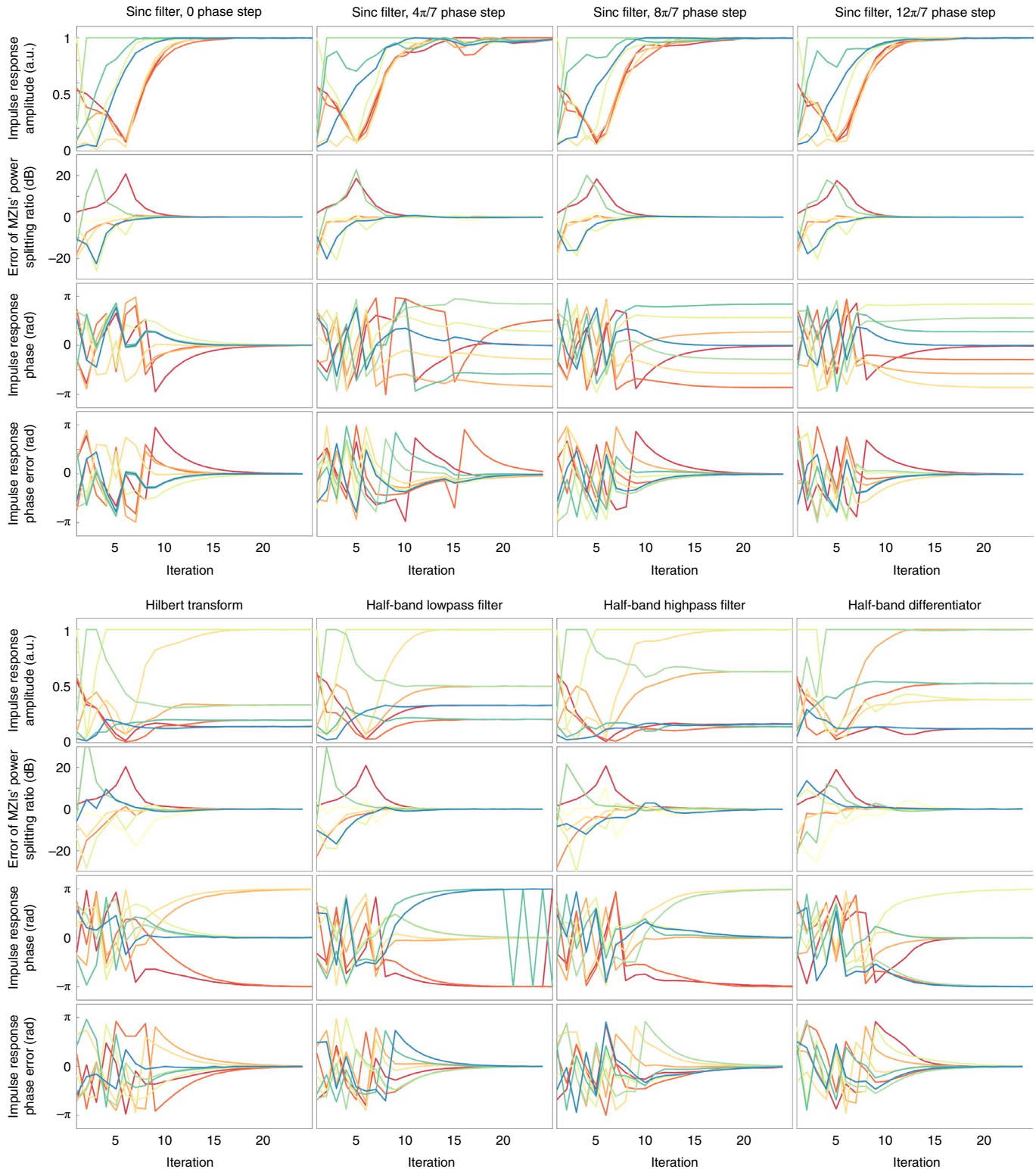

Fig. 3 | The 8-tap signal processing core's parameter evolution during the self-calibration process. The top four columns show the results for complex sinc filters with varying phase steps. The bottom four columns are for a Hilbert transformer, half-band lowpass and highpass filters and a differentiator. The first to fourth rows of each column show the evolution of the 8 taps' amplitudes, the power splitting ratio errors of the MZIs, the 8 taps' phases and the 8 taps' phase errors.

of ϕ_{int} (ranging from π to −π) and the fluctuations of $P_{2\pi}$ (ranging from 0.5 to 0.8 W)—together with the observed thermal cross-talk effects—reveal the challenges during the manual programming of PICs or constructing a look-up table, and thus justify the necessity of a self-calibration method that enables specific functions dialed up on command without prior knowledge of the chip.

The success of our phase recovery methods is verified by: (1) the close match of the impulse response amplitudes obtained

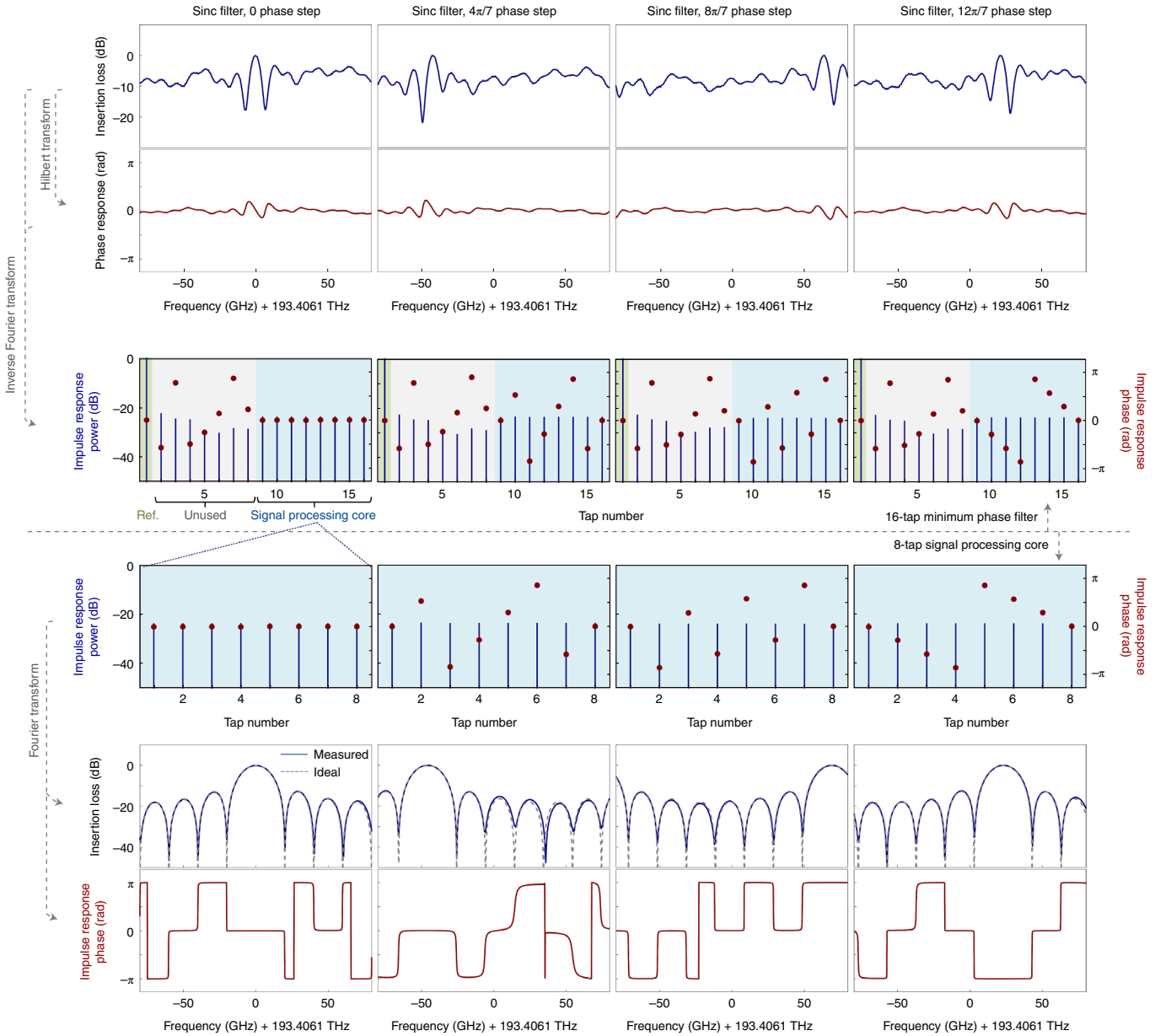

Fig. 4 | Results of self-calibration implementing complex sinc filters. The four columns denote the results of sinc filters with different phase steps between the delay paths. The first to the third rows denote the results for the 16-tap minimum phase filter, including: the measured insertion loss spectra; the phase responses recovered from the insertion loss spectra via a Hilbert transform; and the impulse responses recovered from the frequency responses via an inverse Fourier transform. The fourth to the sixth rows denote the results for the 8-tap signal processing core, including: the impulse responses intercepted from the 16-tap FIR filter's results; the measured and ideal insertion loss spectra; the phase responses recovered from the impulse response via a Fourier transform.

from Kramers–Kronig relationship and measured by an optical vector network analyser (OVA) (Fig. 2j); (2) the relationship between the MZIs' power splitting ratio and the applied electrical power P that matches with the theoretical model (Supplementary Information); and (3) the phase shifters' linear responses to the applied electrical power. As such, the chip's full information can be obtained with our approach for subsequent training of the chip.

Self-calibration process and results. During the self-calibration process, the electrical power applied onto the reference path and unused part of the chip was fixed to maintain the Kramers–Kronig relationship for phase recovery, whereas the electrical power applied onto the 8-tap signal processing core was initially set as zero and trained to dial up the desired functions. The free spectral range of the signal processing core is 160 GHz, set by a 6.25 ps delay increment between adjacent delay paths.

Each training iteration contains several steps: first, the insertion loss spectrum of the 16-tap FIR chip was measured within a single FSR centred at ~1,550 nm, with the wavelength-swept source and power meter; second, the impulse response of the 16 taps was obtained via the phase recovery approach and inverse Fourier transform; third, the power splitting ratios of the MZIs and phase shifts of the phase shifters were recovered from the tap coefficients of the signal processing core and then compared with the desired values to yield errors, which were finally used to update the electrical power applied to the chip. A learning rate of <1 is employed to guarantee the convergence of the learning process.

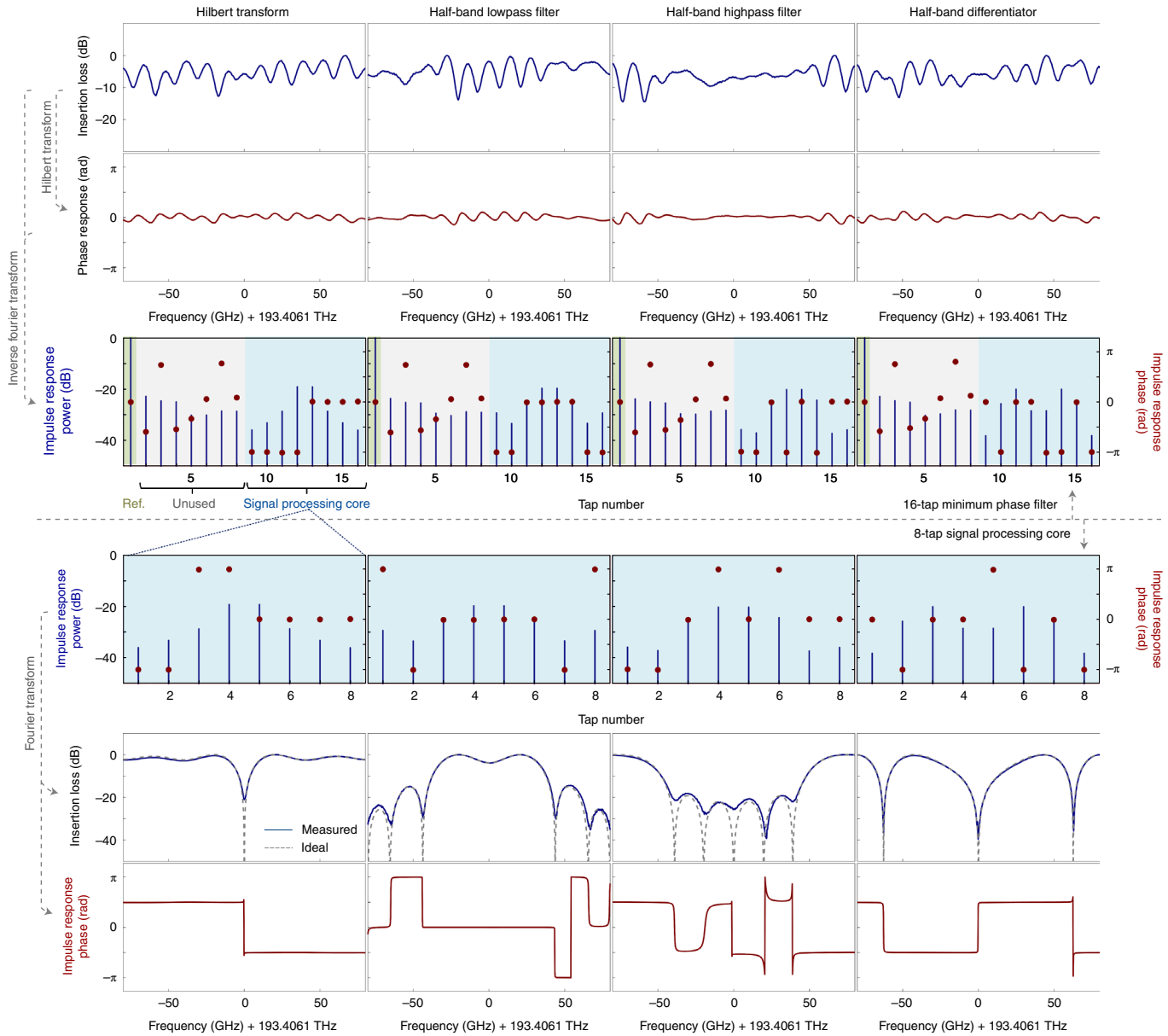

Fig. 5 | Results of self-calibration implementing a Hilbert transformer, half-band lowpass and highpass filters, and a differentiator. The four columns denote the results of different signal processing functions. The first to third rows denote the results for the 16-tap minimum phase filter, including the measured insertion loss spectra, the recovered phase responses and the recovered impulse responses. The fourth to sixth rows denote the results for the 8-tap signal processing core, including the impulse responses intercepted from the 16-tap FIR filter's results, the measured and ideal insertion loss spectra, and the recovered phase responses.

This self-calibration approach brings about two advantageous factors for chip calibration: on the one hand, prior knowledge of the chip, other than designed parameters, is not required—the chip parameters for the learning process (such as $P_{2\pi}$, which varies substantially between different MZIs and phase shifters, was set to 0.75 W herein) do not need to be set as practical values that require time-consuming measurements. On the other hand, the complicated on-chip thermo/electrical cross-talk effects do not need to be addressed using, say, compensating cross-talk matrices, which are time-consuming (and sometimes impossible) to obtain; instead, the thermal cross-talk's impact on the practical chip parameters is taken into account during the calculation of errors (Supplementary Information), and thus mitigated when the calibration iterations converge. Note that due to the MZI's symmetric power transfer function with respect to its phase shift (Fig. 2e), we adopted a two-iteration approach to obtain a rough estimation of the MZIs' initial phase shifts ϕ_{int} for a faster convergence (Methods).

To verify the self-calibration of the 8-tap signal processing core, we now demonstrate diverse transfer functions including complex sinc filters with varying phase steps, a Hilbert transformer, half-band lowpass and highpass filters, and a differentiator. As shown in Fig. 3, the tap coefficients of the FIR signal processing core converged to the desired values and the errors settled to near-zero after 25 self-calibration iterations, where the distinct amplitude and phase distribution of the taps can be observed. The relatively fast convergence of the self-calibration process is a result of the successful recovery of the chip's tap coefficients, which enables direct calculation of the error and updating amounts of electrical power applied onto the chip.

Figures 4 and 5 show the results for different signal processing functions with complex and real tap coefficients after self-calibration. The 16-tap minimum phase filter's insertion loss spectra (that is, the power responses) of a single FSR centred at 193.4061 THz (or 1,550.067 nm) is measured at the self-calibration ports and used to recover the corresponding phase response via a Hilbert transform (Figs. 4 and 5, top two rows), with the corresponding signal processing core's tap coefficients matching with the desired functions. As such, at the signal input/output ports, the desired transfer functions achieved by the signal processing core can be obtained, as shown in the measured insertion loss spectra (Figs. 4 and 5, fifth row), which matched the calculated results, and the recovered phase responses showing the expected phase jumps (Figs. 4 and 5, last row). We note that our device supports wideband operation covering the full optical C band (Supplementary Fig. 12), albeit with perturbations of the taps' phases induced by waveguide dispersion away from the calibrated FSR. In our case, as the employed phase shifters are essentially tunable optical delay lines, they are relatively sensitive to the waveguide dispersion when operating in a broad bandwidth (that is, the optical delays achieved by the employed phase shifters, and thus the tap phases, vary with wavelength). As such, although the tap phases within the calibrated FSR closely match the desired values, the tap phases in distant FSRs are perturbed by the waveguide dispersion. This issue could be addressed by: (1) compensating for the waveguide dispersion with waveguide sections featuring an opposite dispersion value; (2) employing wideband optical phase shifters such as with MRR-based schemes[43] (with the cavity delays matching with the chip's FSR); (3) tailoring the waveguide structures to minimize the dispersion (such as using strip/slot waveguides[44]), or by using banks of filters to cover a large wavelength range.

Conclusion

We have demonstrated a self-calibrating programmable photonic FIR chip, featuring an FIR signal processing core and an integrated path for Kramers–Kronig phase recovery. Our chip offers the capability of recovering phase responses within a broad bandwidth from the amplitude responses, thus obtaining the full amplitude and phase information of on-chip elements for accurate and fast-converging training of on-chip parameters. We use the self-calibration capability to demonstrate diverse signal processing functions including complex-valued sinc filters with varying phase steps, a Hilbert transformer, half-band lowpass and high-pass filters, and a differentiator. This work equips programmable PICs with a powerful capability of dialing-up versatile signal processing functions on demand, which in turn boosts the potential of large-scale integrated photonic chips for applications such as massively parallel neuromorphic computing, quantum computing and optical communications.

Online content

Any methods, additional references, Nature Research reporting summaries, source data, extended data, supplementary information, acknowledgements, peer review information; details of author contributions and competing interests; and statements of data and code availability are available at https://doi.org/10.1038/s41566-022-01020-z.

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Methods

The optical FIR chip was fabricated using TriPleX Si_3N_4/SiO_2 platform (LioniX International)[45,46], with a total chip footprint of 0.9 cm^2. The waveguide uses a double-stripe geometry, where two 1.2 μm × 170 nm stripes of Si_3N_4 are filled with SiO_2, achieving a propagation loss of 0.15 dB cm^{-1}, group index of 1.71 and wavelength dependency of 2×10^{-5} per nanometre (refs. [45,46]). The waveguide features single-mode operation at 1,550 nm and is optimized for transverse electric polarization mode light coupling. Chromium heaters (each with ~600Ω resistance) are used to tune the MZIs and phase shifters via thermo-optical effects, and they are wire-bonded to a carrier printed circuit board to receive external electrical power. The FIR chip consists of: a binary-tree-structured 8 × 16 coupler array with 2 × 2 tunable MZIs, a 16-arm array of linearly incremental delay lines (6.25 ps delay increment) based on S-shaped spiral with a bend radius of 150 μm, and a binary-tree 16 × 8 coupler based on 3 dB directional couplers. This structure offers full control of both amplitude and phase of each optical delay path or tap of the FIR filter. OptoDesigner (PhoeniX Software) was used to layout the chip.

During the experiments, the chip was mounted on an external thermal controller, with the temperature stabilized at 30 °C to compensate for the heat generated by the on-chip phase shifters. We note that the calibration can remain valid for a sufficiently long period with stable electrical power supplies and chip temperature control, and only needs to be performed again when the transfer function of the chip needs to be reconfigured.

The optical insertion loss spectra (that is, the power response or the squared amplitude response) of the chip were measured by an OVA (Luna OVA 5000), which can be replaced with a wavelength-swept laser and an optical power meter, as we introduced above. We note that on-chip forms of the wavelength-swept laser and optical power meter are readily available with state-of-the-art fabrication techniques. The former can be implemented with vertical cavity surface emitting lasers using microelectromechanical structures[47], whereas the latter can be implemented with III–V on silicon platforms[48]. The wavelength scanning range could potentially reach over 150 nm (at 1,550 nm) with a speed of over 10 MHz, which corresponds to a lower limit of ~0.1 μs to the temporal duration of each self-calibration iteration.

As for the setting of the Kramers–Kronig relationship, we employed the impulse response measurement function of Luna OVA 5000 to enable the responses of the unused taps to be removed by time-gating; this would not be necessary if the unused taps were removed in future chips, and can be achieved by simply using a 3 dB coupler that splits the input optical power equally between the reference path and the signal processing core, where the reference path has the shortest path and thus the lowest on-chip loss to sustain the Kramers–Kronig relationship for phase recovery.

To achieve a faster convergence for the self-calibration process, the initial phase shifts of the signal processing core's MZI were roughly estimated. Considering the MZI's symmetric power transfer function with respect to its phase shift (that is, each recovered power splitting ratio corresponds to two possible phase shifts at different slopes), given as:

$$\text{Power splitting ratio} = 10\log_{10}\left(\tan\left(\frac{P/P_{2\pi} \times 2\pi + \phi_{\text{int}}}{2}\right)^2\right),$$

we employed a two-iteration measurement approach, in which the taps' phases were measured twice using the phase recovery approach, with the electrical power applied onto the MZIs as zero and 0.05 W, respectively.

Data availability

The authors declare that the data supporting the findings of this study are available within the paper and its Supplementary Information.

Code availability

The authors declare that the algorithm supporting the findings of this study are available within the paper and its Supplementary Information.

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Author contributions

X.X., A.J.L. and A.B. conceived the idea and designed the project. X.X. performed the numerical simulations and experiments. G.R., A.B. and T.F. prepared experimental hardware. X.X., A.J.L., A.B., G.R., X.L. and A.M. contributed to the development of the experiment and to the data analysis. X.X. and A.J.L. wrote the manuscript with inputs from all other authors. A.J.L. and A.B. supervised the research.

Competing interests

The authors declare no competing interests.

Additional information

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