

# Logic Gates of Terahertz Spoof Surface Plasmons

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Spoof surface plasmon polariton (SSPP) interconnects have great potential for the next-generation wireless communications and terahertz (THz) integrated circuits. SSPP logic gates are reported to meet the above development requirements. However, the reported SSPP logic gates consist of 3D domino waveguide structure and conversion structure with a funnel-shaped metasurface; and hence, suffer from the size limit of the compact on-chip integrations. To explore a more compact and flexible design, a series of logic gates in the planar THz SSPP platform, including OR, AND, XOR, NOT, and NAND gates, is experimentally demonstrated. Owing to the flexible dispersion behaviors, different phase differences between inputs can be controlled by manipulating the SSPP waveguide structure, such as the SSPP Mach–Zehnder interferometer, thereby realizing various THz SSPP logic gates, which will enable powerful potential in large-scale on-chip systems, future wireless communications, and intelligent computing.

## 1. Introduction

With the increasing demand for ultrahigh-speed wireless communication, the terahertz (THz) technology holds great potential for developing next-generation communications systems due to its ultra-bandwidth, faster processing speed, and greater data transfer rate.<sup>[1–7]</sup> To realize high-speed information transfers, the interconnects play a vital role in intra-chip and inter-chip communication links. In the THz frequency, the communication bandwidth of traditional electrical interconnection is limited by RC delay.<sup>[8,9]</sup> Optical interconnects can tackle this limitation owing to higher information-carrying capacity. However, the diffraction limit and the complicated electro-optical signal conversion have restricted its development.<sup>[9–11]</sup>

A promising approach to break through the limits of electrical and optical interconnects in the THz region is the spoof surface

plasmon polariton (SSPP) interconnects.<sup>[9]</sup> First reported by Pendry in 2004, SSPPs are electromagnetic surface waves at THz and microwave frequencies, supported by metal conducting surfaces perforated by holes.<sup>[12]</sup> SSPPs inherit the characteristic of strong field confinement of optical SPPs and further push the diffraction limit.<sup>[12–19]</sup> Compared to SPPs, SSPPs have a smaller ohmic loss.<sup>[20]</sup> Subsequently, the SSPP structure has changed from bulk to planar to facilitate engineering applications.<sup>[21]</sup> In order to excite the surface waves, high-efficiency conversion structures are reported.<sup>[22,23]</sup> Benefitting from the strong field confinements and easy integration, the SSPP signals can be transmitted efficiently when the SSPP waveguide structures are placed in parallel,<sup>[9,24–27]</sup> which lays the foundation for the next generation of inter-chip


communications. Thereafter, some SSPP-based devices were explored in microwave waves.<sup>[28–32]</sup>

In order to satisfy the development requirement of next-generation communication, some THz devices and logic gates are necessary. In particular, the logic gates are critical in integrated circuits for switching, digital processing, and computing.<sup>[33–36]</sup> Recent advances in SSPPs have opened an efficient route to realize the THz on-chip compact devices with desired functionalities. For example, some SSPP-based THz devices have been reported and experimentally demonstrated, such as filters, power dividers, couplers, splitters, switchers, and logic gates.<sup>[37–43]</sup> However, the above-mentioned THz SSPP-based logic circuits with domino-like metallic structures consisting of a periodic chain of domino-shaped elements are difficult to be integrated compactly into on-chip systems.<sup>[43]</sup> Therefore, mass scaling of such architecture in chips will be a huge challenge. Moreover, additional excitation and focusing structures need to be integrated into the logic circuit<sup>[43]</sup> in order to realize the wavevector match between the spatial THz wave and SSPPs, which will further increase the difficulty of minimization and integration.

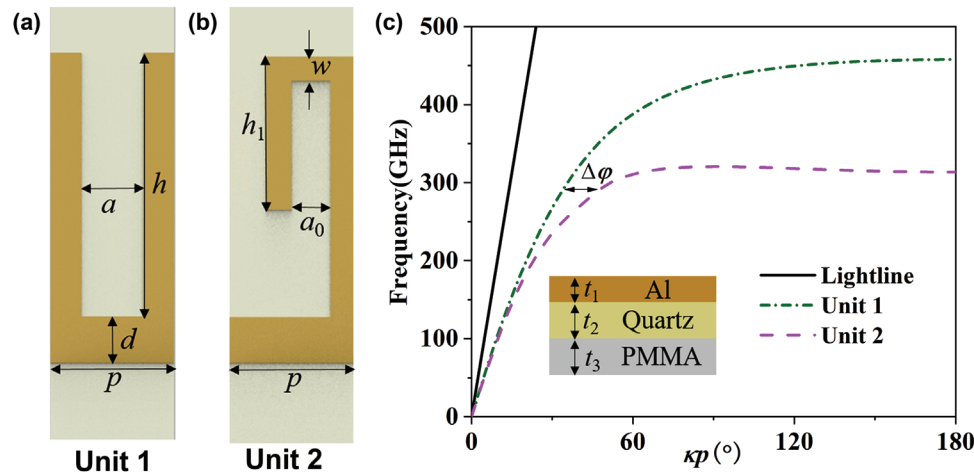
Here, we propose and experimentally demonstrate a series of THz logic gates in a planar SSPP system to make this approach suitable for on-chip integration and communications. The phase difference between the upper and lower arms of the SSPP logic circuits, similar to the Mach–Zehnder interferometer, can be controlled by manipulating the dispersion behavior. The OR and AND gates are realized when the phase differences are the same. Then, by changing the SSPP structure, the phase difference is switched from 0 to  $\pi$ , and XOR and NOT

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 The ORCID identification number(s) for the author(s) of this article can be found under <https://doi.org/10.1002/admt.202201225>.

DOI: 10.1002/admt.202201225



**Figure 1.** a,b) The structural diagrams of SSPP units 1 and 2, respectively, where the structural parameters are  $p = 40 \mu\text{m}$ ,  $h = 85 \mu\text{m}$ ,  $d = 15 \mu\text{m}$ ,  $a = 20 \mu\text{m}$ ,  $a_0 = 12 \mu\text{m}$ ,  $w = 8 \mu\text{m}$ , and  $h_1 = 50 \mu\text{m}$ . c) Dispersion relations of unit 1 and unit 2. Note that the SSPP unit with Al metal of the thickness of  $t_1 = 0.3 \mu\text{m}$  is etched on the quartz substrate with the thickness of  $t_2 = 120 \mu\text{m}$ , and the bottom layer is the PMMA with a thickness of  $t_3 = 2000 \mu\text{m}$ .

are obtained. In addition, a hybrid SSPP structure achieves the NAND gate by cascading the above two logic circuits. These compact SSPP logic circuits are planar rather than 3D, satisfying the requirements of future applications in the on-chip integrations and wireless communications.

## 2. Theory and Analysis

The terahertz (THz) SSPP unit structures with Al metal (the thickness  $t_1$  is  $0.3 \mu\text{m}$ ) are shown in **Figure 1a,b**, where they are etched on the quartz substrate with the thickness of  $t_2 = 120 \mu\text{m}$ , the permittivity constant of  $\epsilon_r = 3.75$ , and the loss of  $\tan \delta = 0.0004$ . The structure's bottom layer is the PMMA material with a thickness of  $t_3 = 2000 \mu\text{m}$ . In addition, the structural parameters are  $p = 40 \mu\text{m}$ ,  $h = 85 \mu\text{m}$ ,  $d = 15 \mu\text{m}$ ,  $a = 20 \mu\text{m}$ ,  $a_0 = 12 \mu\text{m}$ ,  $w = 8 \mu\text{m}$ , and  $h_1 = 50 \mu\text{m}$ . Compared with unit 1, unit 2 has a deeper groove depth, denoting that they have different wavevectors. This characteristic can be demonstrated by their dispersion behaviors, as shown in **Figure 1c**.

The Eigenmode simulation can obtain the dispersion behaviors in the commercial software CST. As the frequency increases, the dispersion curves increasingly move away from the light line, and the wavevectors also gradually increase. Then, they tend to have different cutoff frequencies. Due to a deeper groove depth, unit 2 has a larger wavevector than unit 1 at the same frequency. Their phase difference gradually increases as the frequency increases. The corresponding phase difference can be expressed as

$$\Delta\varphi = \varphi_2 - \varphi_1 \quad (1)$$

where,  $\varphi_1$  and  $\varphi_2$  denote the phases of units 1 and 2, respectively. Thus, owing to the flexible dispersion behaviors of SSPP, the phase difference can be realized by manipulating the SSPP unit structure. The phase difference between the SSPP structures consisting of units 1 and 2 is

$$\Delta\varphi_0 = n_2\varphi_2 - n_1\varphi_1 \quad (2)$$

where  $n_1$  and  $n_2$  are the numbers of units 1 and 2, respectively. The phase difference depends on the number and the phase of units. Thus, different phase differences can be realized by changing the SSPP structural parameters. We can also observe from the dispersion curves that the phase difference and attenuation will be at their maximum as the frequency approaches the cutoff. Thus, a balance between the attenuation and phase difference also needs to be considered to realize the high-efficiency transmission performance.

Two ground-signal-ground (GSG) probes are used for the THz measurements to excite and receive the THz signal waves. Due to the limitations of the experimental conditions, the proposed SSPP waveguide structure is designed to be similar to the Mach-Zehnder Interferometer (MZI), where the upper and lower arms are regarded as the two input signals, respectively.<sup>[44,45]</sup> Thus, the phase difference ( $\Delta\varphi_0$ ) between the upper and lower arms determines the output state and can be written as

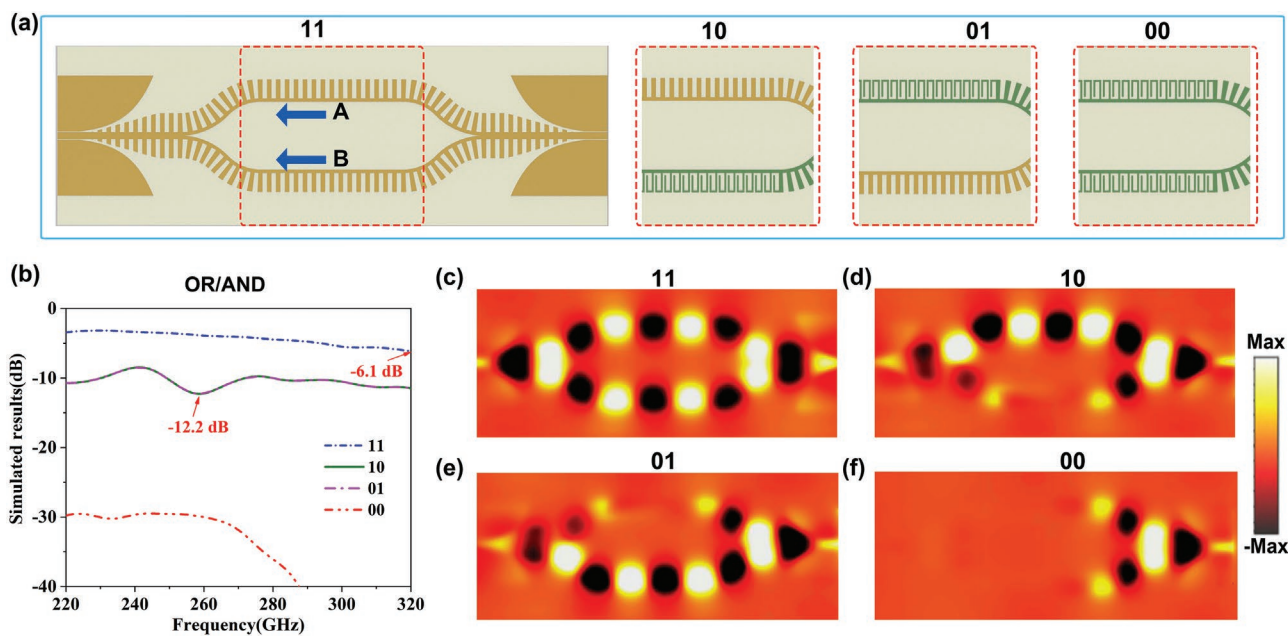
$$|A_o| = \left| A_i \cos \frac{\Delta\varphi_0}{2} \right| \quad (3)$$

where  $A_o$  and  $A_i$  are the output and input amplitudes of the waveguide, respectively. When the phase difference is  $(2k + 1)\pi$  ( $k = 0, \pm 1, \pm 2, \dots$ ), the output signal is zero. On the contrary, when the phase difference is  $2k\pi$ , the output energy equals the input energy. Here, the  $0$  and  $\pi$  phase differences are analyzed to realize different logic gates. For the SSPP structure, owing to its flexible dispersion behaviors, various phase differences can be obtained by constructing its structure, thereby realizing the output in different states.

## 3. Design and Results

### 3.1. OR/AND Gate

When the terahertz (THz) signal is injected into the SSPP waveguide from right to left, the input signal is equally divided into

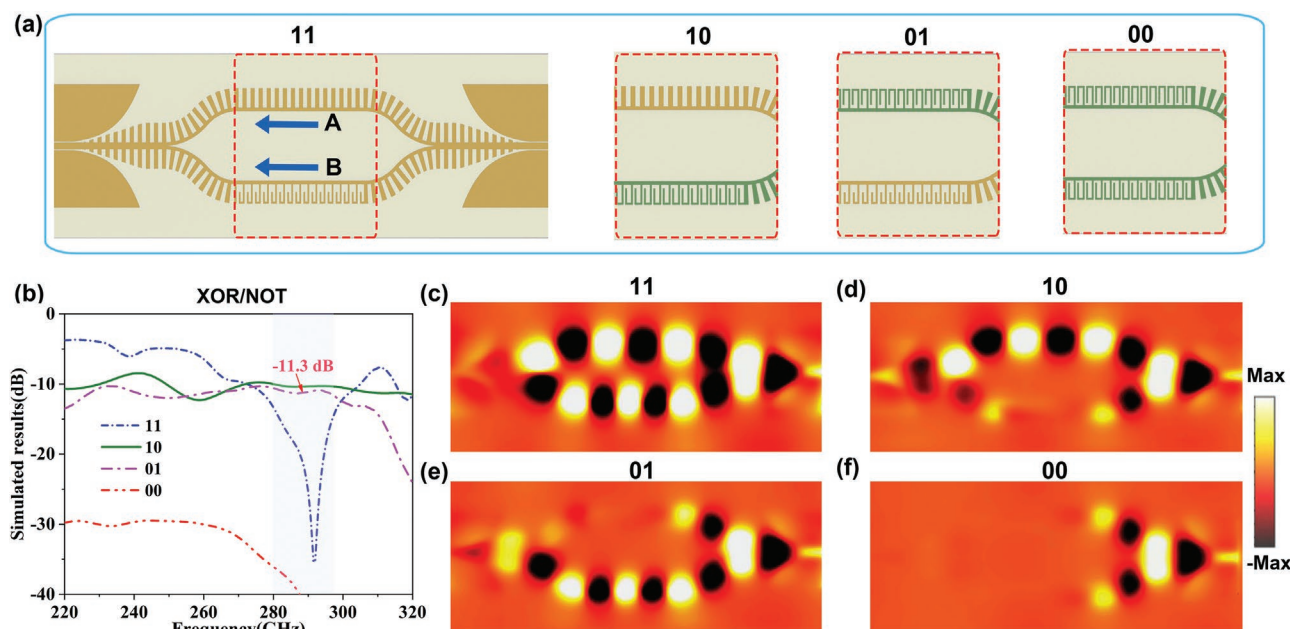


**Figure 2.** Logic operation of OR/AND. a) SSPP structures in the four states where the SSPP structure with the length of 2458  $\mu\text{m}$  in the red dotted-line block diagram is redesigned to realize different inputs. b) Simulated transmission parameters. c–f) Simulated near electric-field distributions corresponding to four states at 290 GHz. Note that in order to realize the zero input, the SSPP structure with Al metal (yellow) is replaced by the different SSPP structure with Ni metal (green). In addition, the THz signal is injected from the right of the SSPP structure.

the upper and lower paths (A and B), as shown in Figure 2a. In order to excite the SSPPs with high efficiency, the corresponding conversion structure is also designed (for details, see Section S1, Supporting Information). The upper and lower arms (A and B) are regarded as two different signal channels of the logic gates. More importantly, owing to the strong field confinement of SSPPs, the input signals can be transmitted almost without crosstalk (see Section S2, Supporting Information). Here, in order to mimic the zero input, the corresponding arm with Al metal (yellow) is replaced by the SSPP structure with Ni metal (green), where the structural parameters are  $a_0 = 17 \mu\text{m}$  and  $h_1 = 70 \mu\text{m}$ . Owing to low conductivity and high permeability, Ni metal can enlarge the metal loss and prevent signal transmission.<sup>[31]</sup> The SSPP structures in four different input states (“11”, “10”, “01”, and “00”) are constructed. The corresponding simulated transmission parameters as the frequency varying from 220 to 320 GHz are illustrated in Figure 2b. When the input signal is “11” state, the output amplitude is higher than in the other states. Owing to the structural symmetry, the “10” and “01” states have the same output. In addition, in order to more intuitively observe the corresponding outputs in different inputs, the near-field distributions at 290 GHz are simulated, as illustrated in Figure 2c–f. We can clearly observe that Ni metal can prevent the transmission of electromagnetic waves. Compared with the “10” and “01” states, the output energy in the “11” state is the maximum. When the input has no signal, the corresponding output is zero. In addition, different logic gates can be obtained by defining output thresholds. The output is zero when the threshold value is lower than  $-18 \text{ dB}$ , and the OR logic gate can be obtained; the output is zero when the threshold value is lower than  $-6.5 \text{ dB}$ , and the AND logic gate can be realized within 220–320 GHz.

### 3.2. XOR/NOT Gate

For the XOR gate, the output is zero when the input signals are high level. Equation (3) shows that the output is zero when the phase difference between the upper and lower arms reaches  $\pi$ . Owing to the flexible SSPP dispersion behaviors, the  $\pi$  phase difference can be realized by manipulating the structural parameters, thereby realizing a zero output. From the dispersion curves shown in Figure 1c, when the operating frequency is 290 GHz, the phase difference between units is  $\Delta\varphi = \pi/16$ . Thus, when the number of unit 2 is  $\approx 16$ , a  $\pi$  phase difference between the upper and lower arms consisting of units 1 and 2 can be realized at  $\approx 290 \text{ GHz}$ , as shown in Figure 3. Similarly, the zero input can be obtained by introducing the Ni metal. The simulated transmission parameters are shown in Figure 3b. As expected, when the input signals are “11” state, the output of the SSPP waveguide is zero at  $\approx 290 \text{ GHz}$ . When the input signals are “10” and “01” states, their transmission parameters are basically the same and can reach  $\approx -11 \text{ dB}$ . Near-field distributions at 290 GHz can also intuitively display the output information in different input states, as shown in Figure 3c–f. When the input signal is “11” state, we can clearly observe that the upper and lower arms have 3.5 and 4 operating wavelengths, respectively. Thus, a  $\pi$  phase difference is obtained, and the output is zero. Note that an SSPP switcher can also be realized by switching the lower arm of the SSPP structure, as shown in Figures 2b and 3b. In order to obtain a logic gate, a transmission threshold needs to be set. The output is zero when the transmission threshold is lower than  $-18 \text{ dB}$ ; and thus, an XOR gate can be realized within 280–297 GHz. In addition, the NOT logic gate can be obtained when the upper or lower arm is used as the control signal line.



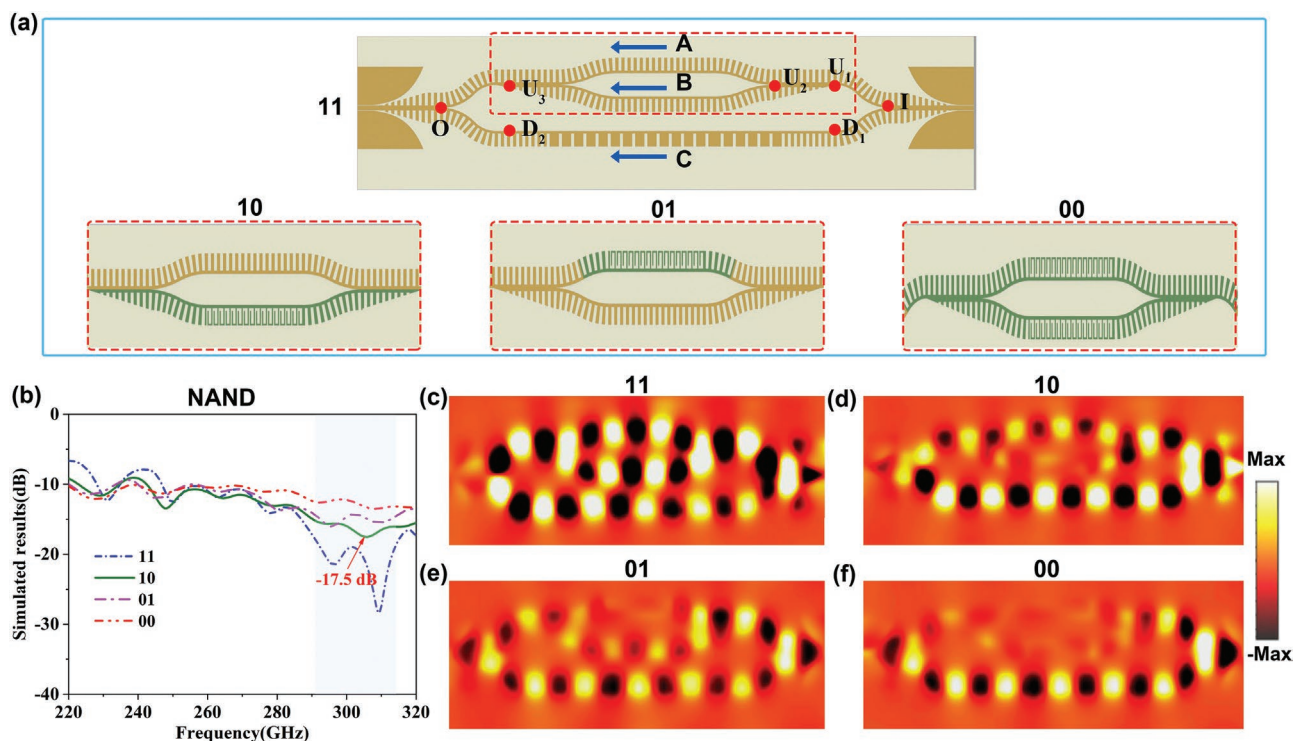
**Figure 3.** Logic operation of XOR/NOT. a) SSPP structures in the four states where the SSPP structure in the red dotted-line block diagram is redesigned to realize different inputs. b) Simulated transmission parameters. c–f) Simulated near electric-field distributions corresponding to four states at 290 GHz.

### 3.3. NAND Gate

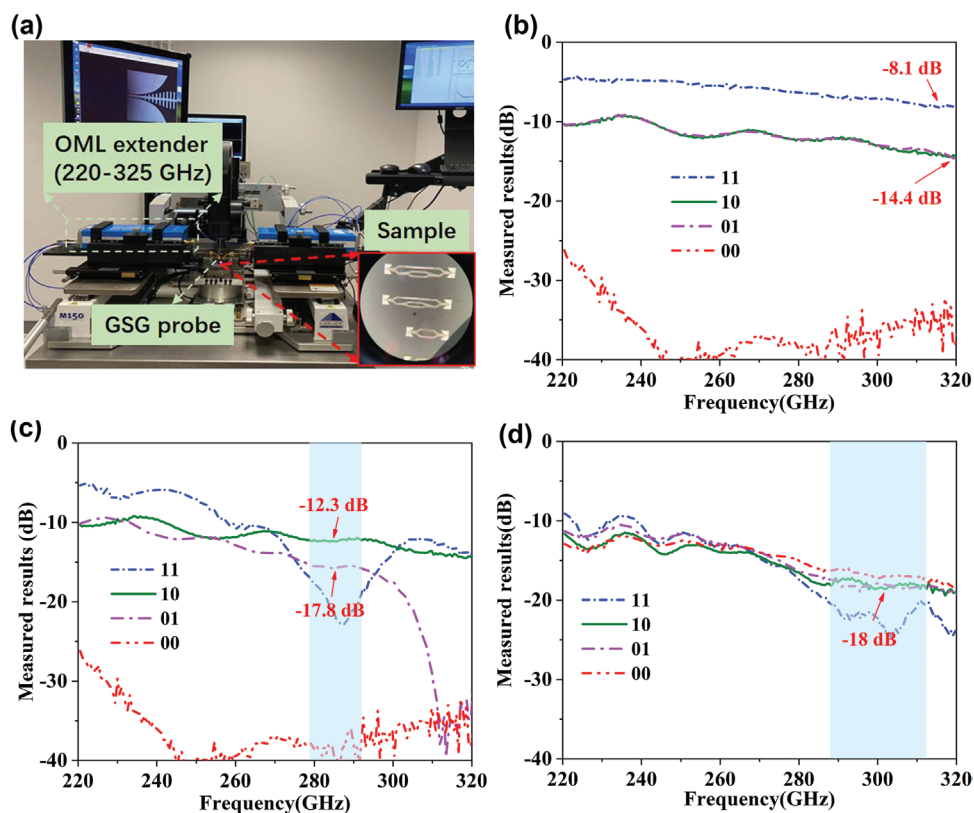
In terms of the above analysis, the AND and NOT gates can be implemented by manipulating the structural parameters in the SSPP MZI-like configuration. Compared to the fundamental logic gates (OR/AND and XOR/NOT gates), NAND gate is more complicated. Here, a complex NAND logic gate can be constructed by cascading the two different SSPP MZI-like waveguides (AND and NOT), as shown in **Figure 4a**. Similarly, the signal wave is also injected from the right of the SSPP structure. When the input wave reaches point I, the energy is equally divided into two paths marked as points  $U_1$  and  $D_1$ . The transmitted energy marked as point  $U_1$  is further divided into two input paths (A and B) after reaching point  $U_2$ . Here, the A and B paths are regarded as the input signals of the logic gate. The transmitted energy reaching point  $D_1$  will be transmitted along the control line (C), whose transmission energy remains a constant. The control line and the upper SSPP structure consisting of the A and B paths have a  $180^\circ$  phase difference. Thus, the output at point O is zero when the input signals are in the “11” state. When the input signals are in the “10” state, the output at point O is high (or 1). It is because the ratio of their energies is close to 1:2; although, the phase difference between points  $U_3$  and  $D_2$  is close to  $\approx 180^\circ$ . Similar to the “10” state, the output at point O is high in the “01” state. When the inputs are in the “00” state, the transmitted energy at point  $U_3$  is almost zero. Thus, the output energy at point O is approximately equal to the transmitted energy of the control line. Here, the structural parameters of the unit structure of the control line are  $p = 80 \mu\text{m}$  and  $a = 20 \mu\text{m}$ , and the number of units is 19. Meanwhile, the signal energy at the upper path reaches point 2 and is equally divided into two paths (A and B) again. The two paths A and B are regarded as the two input sig-

nals, which can be adjusted by manipulating the metal forms of the SSPP structure, as shown in **Figure 4a**. The transmission parameters in four input states are simulated (**Figure 4b**). When the inputs are in “11” states, the output is zero at  $\approx 310$  GHz due to a  $\pi$  phase difference between the input and the control lines. When the input signals are in “10” or “01” states, the output corresponding outputs are the superposition of the energy of the signal line A or B and the control line C, respectively, and their outputs are approximately equal. Compared with the output energy in the “10” and “01” states, the transmission performance in the “00” state is better. The simulated near-field distributions can intuitively display the above results as shown in **Figure 4c–f**. As shown in **Figure 4c**, the phase of the lower arm is  $\approx \pi$  smaller than that of the upper arm, so the output is zero. By comparison, the output of the SSPP structure in the other states is larger. The output is zero when the threshold is lower than  $-18$  dB. Thus, the NAND logic gate can be achieved at  $\approx 291$ – $315$  GHz.

In order to verify the simulated results for different logic gates, the THz experimental measurement platform is set up, as shown in **Figure 5a**. The working frequency range is from 220 to 325 GHz with the OML extenders. Here, the samples are fabricated by lithography and excited by a GSG probe, respectively. Then, the transmission signals are received by the other GSG probe. The measured transmission parameters are illustrated in **Figure 5b–d**. The measured transmission parameters when the upper and lower arms of the SSPP structure with two input ports are the same, are shown in **Figure 5b**. Compared with the simulated transmission parameters, the measured transmission parameters are reduced by  $\approx 2$  dB mainly due to the manufacturing error, the metallic surface roughness, and large material loss. The OR and AND gates can be realized when the output thresholds are smaller than  $-18$  dB



**Figure 4.** Logic operation of NAND. a) SSPP structures with a length of  $4037 \mu\text{m}$  in the four states where the SSPP structure in the red dotted-line block diagram is redesigned to realize different inputs. b) Simulated transmission parameters. c–f) Simulated near electric-field distributions corresponding to four states at 310 GHz.



**Figure 5.** Measured results. a) The terahertz experimental measurement setup employed to measure the transmission parameters of SSPP waveguides. b) OR/AND gate. c) XOR/NOT gate. d) NAND gate.

**Table 1.** OR/AND at 290 GHz.

Input amplitude	Output amplitude	Threshold amplitude (T)	OR	AND <sup>a)</sup>
1	1	OR ( $T \leftarrow 18$ dB) AND ( $T \leftarrow 10$ dB)*	1	1
1	0	–	1	0
0	1	–	1	0
0	0	–	0	0

<sup>a)</sup>For “AND” logic gate, an attenuation of  $\approx 8$  dB can be introduced into the output port to obtain the same threshold value as the other logic gates.

and  $-10$  dB at  $\approx 220$ – $320$  GHz, respectively. Note that in order to obtain the same threshold value, the attenuation of  $\approx 5$  dB can be introduced into the output port of the “AND” logic gate, where a metal with low conductivity can be introduced to act as an attenuation. The measured transmission parameters when the upper and lower arms of the SSPP structure with two input signals are different and their phase difference reaches  $\pi$ , are shown in Figure 5c. For the lower arm consisting of unit 2, the working frequency is close to the cut-off frequency of the SSPP structure (see Figure 1c). When there is a manufacturing error, the measured results in the “01” state will show a more pronounced difference compared to the simulated results. However, the overall trend is consistent. The XOR and NOT gates can be realized when the output thresholds are smaller than  $-18$  dB at  $\approx 279$ – $292$  GHz, respectively. As shown in Figure 5b,c, when the inputs are in the “11” state, an SSPP switcher is implemented by switching the lower arm of the SSPP structure. Moreover, the SSPP structure consisting of the two inputs and one control line is measured as shown in Figure 5d. It can be clearly observed that compared with the other three states, the transmission parameters in the “11” state are lower and can reach  $\approx -25$  dB at 303 GHz, denoting that the  $\pi$  phase difference between the signal and control lines is achieved. As expected, the transmission parameters are almost the same in the “10” and “01” states, and the transmission parameters in the “00” state can reach the maximum. When the output threshold is lower than  $-18$  dB, the NAND is realized at  $\approx 285$ – $313$  GHz. According to the above analysis, the measured and simulated results have a good consistency. In addition, it can be seen that different logic gates have overlapping operating frequencies. The truth tables of different logic gates when the working frequency is 290 GHz, are shown in **Tables 1–3**. Note that, for the “AND” logic gate, an attenuation of  $\approx 8$  dB can be introduced into the output port to obtain the same threshold value

**Table 2.** XOR/NOT at 290 GHz.

Input amplitude	Output amplitude	Threshold amplitude (T)	XOR	NOT
A	B			
1	1	XOR ( $T \leftarrow 18$ dB) NOT ( $T \leftarrow 18$ dB and B is the control line)	0	0
1	0	–	1	1
0	1	–	1	1
0	0	–	0	0

**Table 3.** NAND at 290 GHz.

Input amplitude <sup>a)</sup>			Output amplitude	Threshold amplitude (T)	NAND
A	B	C			
1	1	1	$-22.1$ dB	$T \leftarrow 18$ dB	0
1	0	1	$-17$ dB	–	1
0	1	1	$-17$ dB	–	1
0	0	1	$-16$ dB	–	1

<sup>a)</sup>Note that A, B, and C are the two input signals, and a control signal, respectively.

as other logic gates. The fundamental logic gates have been demonstrated experimentally in the THz spoof plasmonic platform. Compared with other logic gates consisting of domino structures or graphene, the proposed SSPP logic gates are easy for system integration and small in size (see Section S3, Supporting Information). Hence, we believe that the proposed work will have potential applications in the THz plasmonic metamaterials and communication systems.

## 4. Conclusion

We demonstrated THz SSPP logic gates “OR/AND,” “XOR/NOT,” and “NAND,” and both simulated and experimental results verified that these logic gates could be realized. The spoof plasmonic logic circuits are realized on a planar platform, promising for on-chip integration with THz circuits. Due to SSPP dispersive behaviors’ flexibility, different phase differences between two inputs can be controlled by changing the SSPP structure. In addition, in order to mimic the zero input, the Al metal is replaced by the Ni metal. When the phase difference between two inputs is zero, the OR and AND can be realized by defining the output threshold. Similarly, the XOR and NOT can be obtained, when the phase difference between two inputs is  $\pi$ . A NAND gate is achieved by cascading SSPP structures. We believe this work will expand the scope of plasmonic metamaterials and establish a foundation for THz wireless communication engineering.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

## Acknowledgements

This work was supported in part by the Hong Kong Research Grants Council under Grant T42-103/16-N; the National Key Research and Development Program of China under Grant Nos. 2017YFA0700201, 2017YFA0700202, and 2017YFA0700203; and the Major Project of Natural Science Foundation of Jiangsu Province (BK20212002).

## Conflict of Interest

The authors declare no conflict of interest.

## Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

## Keywords

logic gate, on-chip integrated devices, spoof surface plasmon polaritons, terahertz

Received: July 25, 2022  
Revised: October 11, 2022  
Published online:

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